NAME

kmc − KMC11/DMC11 microprocessor

DESCRIPTION

The files **kmc?** are used to manipulate the KMC11 or DMC11 microprocessors. The only KMC11 currently supported is the KMC11-B. The device handler provides the basic mechanism needed to load, run, and debug programs on the microprocessor.

The open is exclusive; at most one open at a time is allowed. The first open can determine whether the microprocessor is a KMC11 or DMC11 by testing for bit 8 of the microprocessor memory address register; however, this test is disabled in the current implementation, and a KMC11-B is assumed.

Addresses 0−8191 (2047 for the DMC) reference the 4096 (1024 for DMC) words of instructions in the control memory of the microprocessor. For the KMC11, they may be read or written; for the DMC11, they are read-only. This portion is word oriented, that is, the address and byte count must be even.

Addresses 8192-12287 (2048-2303 for DMC) reference the 4096 (256 for DMC) bytes of data in the data memory of the KMC11. The data portion may be read or written with no restrictions on addressing.

The ioctl function is used to provide access to the basic microprocessor capabilities.

```
ioctl(kmcfd, KIOCSETD, argkmcbuf)
struct  {
        int     code;
        int     *csr;
        int     value;
} *kmcbuf;
```

The pointer *csr* contains the address of a 4 word buffer for the UNIBUS Control and Status Registers associated with the microprocessor. The value of *code* determines the function:

1 single step and return CSRs in *csr*.
2 maintenance step: execute *value* and then return CSRs.
3 return CSRs.
4 stop: clear the run bit.
5 reset: set then clear the master clear bit.
6 run: set the run bit and set the software state to *value* and running.
7 line unit maintenance: set the line unit bits from *value*.

FILES

/dev/kmc?

SEE ALSO

kasb(1), kunb(1).