SMALL SYSTEM DIGITAL INPUTS

TABLE OF CONTENTS

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INTRODUCTION

The Small System Digital Inputs hardware provides a means by which the system program can read the status of up to 16 logic variables (yes/no, true/false, set/reset, open/closed, on/off) from various process devices such as switches, valves, relays, and motors. The status of the 16 input lines is read into the processor by two consecutive Read Data instructions. The first Read Data instruction, transfers data from the most significant 8-bit byte of digital inputs and the second Read Data instruction executed transfers the least significant data byte. An external interrupt point is provided, which when enabled by a customer connection, will generate an interrupt which may be used to inform the program that the digital inputs should be read. An external busy input signal may also be implemented and monitored by the Sense Status instruction. The busy input is temporarily grounded to inform the program that valid digital inputs are present and should be read.

In some applications, Change Detection input termination circuits may be implemented which provide a signal to an Interrupt Module to inform the program when the status of any of the 16 inputs change state.

Functional Description

Fig. 1 illustrates the Small System Digital Inputs hardware in block diagram form. This figure illustrates the basic signal flow and lists the model numbers of the functional modules that make up the subsystem. All Small System Digital Inputs hardware modules are normally located within the Central System Cabinet (CSC).

The 4DP3000AF1201 Sense Line Module consists of a standard 9.75 inch by 10.5 inch mother board. The board may be installed in any available slot on the Computer's Multiplexer Bus. The Sense Line Module is normally assigned address X'11', however, this address may be changed by jumper wiring on the

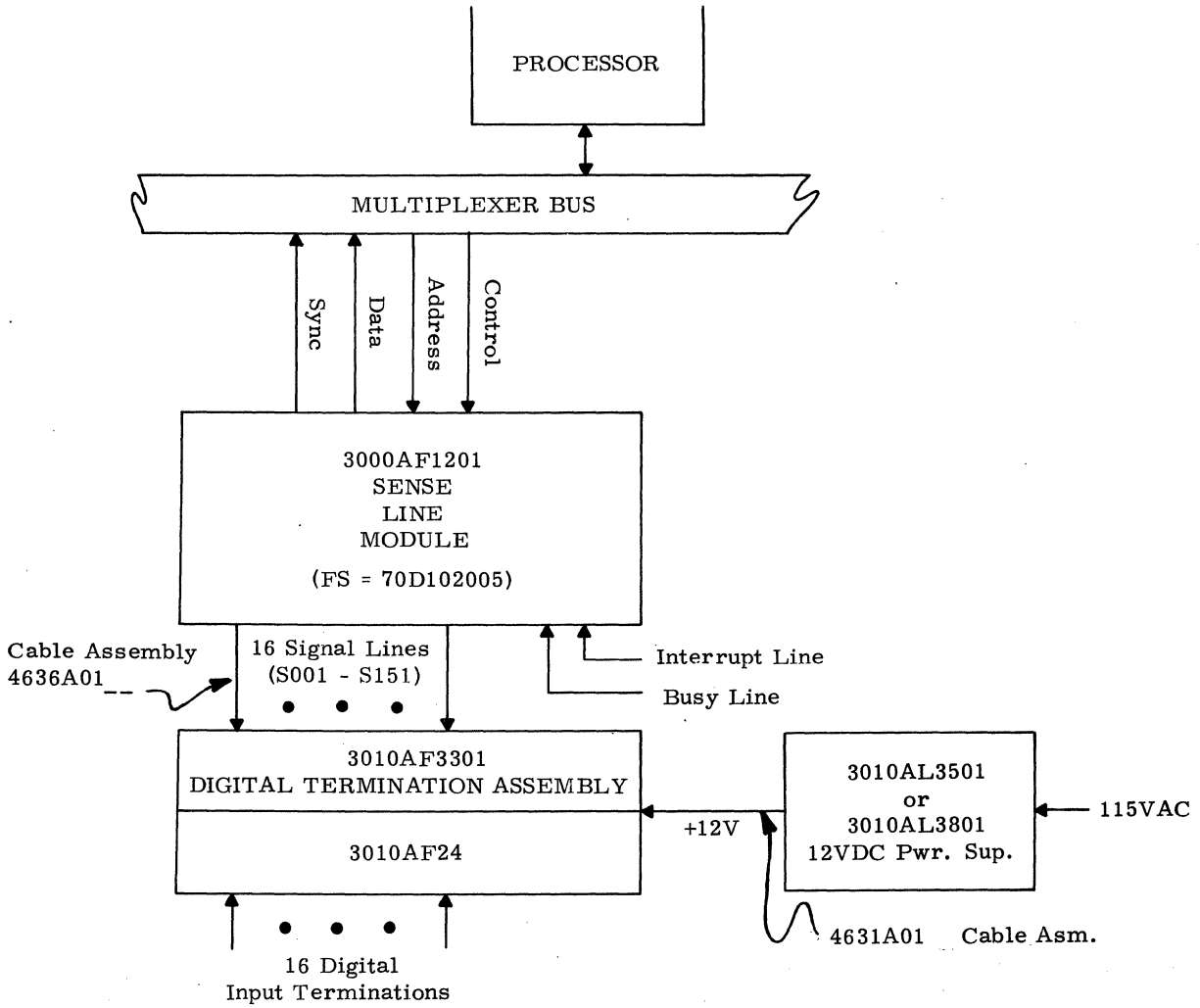

Fig. 1 Small System Digital Inputs

mother board. The Sense Line module accepts 16 digital input signals, an external interrupt signal, and an external busy signal.

The status of the 16 digital input signals is read into the processor by two consecutive Read Data instructions. The status of the input lines is gated directly through to the processor by the Read Data instruction and not stored in the Sense Line Module.

The externally controlled interrupt line, when enabled, will generate a computer interrupt which may be used to initiate the proper subroutine for reading the digital inputs, checking them, etc. This interrupt can be armed and disarmed under program control using Output Command instructions.

The external busy line may be used to inform the program when the digital inputs are valid and should be read. Execution of the Sense Status instruction monitors the status of this line.

The 4DP3010AF3301 Digital Termination Assembly permits connections from the process via screw-type terminals, and provides card slots for 4DP3010AF24xx Buffer Relay boards that adapt the process inputs to the Sense Line Module. Each Buffer Relay board contains circuits for 8 digital input points. The Basic Digital Termination Assembly permits 16 circuit terminations. This assembly will support add-on terminations which may be expanded in 16 circuit increments up to a maximum of 80 circuits, using the 3010AF3303 Input Adder Assemblies. Each 16 digital input termination requires a separate Sense Line Module. The Termination Assembly may also be used for external interrupt connections to an Interrupt Module.

The Buffer Relay boards are powered by a 4DP3010AL3501 (1 amp.) or 4DP3010AL3801 (5 amp.) 12 VDC Power Supply.

References

In addition to the Theory of Operation described in this publication, the following documents are provided to support the Small System Digital Inputs hardware:

- Functional Schematics

  Sense Line Module - 71D102005 (Previously 70B113242 or FS32)

  3010AF2401 Buffer Relay board - PX3600IHSL1

- Maintenance

  3000AF12-M located in the Digital I/O section of the GE-PAC 3010 Computer Maintenance Manual.

- Hardware Location/Address/System Connections

  System Configuration Drawing - Unique for each system (Referenced on the System Model List - 4DP0005ASID)

- Reference Manuals

  GE-PAC 30/3010
  Reference Manual - GET-6047
  Systems Interface Manual - PCP 126

  GE-PAC 3010/2
  Central Processor Reference Manual - GET-6174

- Illustrated Parts

  Illustrated Parts section of the GE-PAC 3010 Computer Maintenance Manual. (Sense Line Module mother board assembly is 32-070. Parts for the Relay Buffer printed wiring boards are provided on the schematic for the board, e.g., PX3600IHSL1.)

- 12 Volt Power Supply

  Refer to the System Power section of the GE-PAC 3010 Computer Maintenance Manual.

- Wire Lists

  Digital Input Termination Assembly - 70A121688
  Cable, Control Line Module to Termination assembly (4636A02xxx) - 70A122003P1
  Cable, Power (4631A01xxx) - 70A121175

> NOTE
>
> The last three digits (xxx) of cable model numbers corresponds to the cable length in feet.

- Test Program

  Sense Line Module Test - 70A112464

Options

ADDRESS

The address for the Small System Digital Inputs subsystem is normally wired for X'11'. This address may be selected for any address from X'00' to X'FF' by changing the positions of wire jumpers on the Sense Line Module. The only restriction is that the address selected must not duplicate the address of any other I/O Controller on the Multiplexer Bus.

The logic elements which select and decode the address are shown on sheet 1 of the Sense Line Module

functional schematic. The address is selected by means of wire wrap jumpers at position 20 on the Sense Line Module mother board. Table 1 shows the function of each jumper pin and lists the actual connections for several different addresses, including the normal address, X'11'.

The address of the module, as shipped from the factory, is listed on the System Configuration drawing.

TERMINATION BOARDS

Various types of Buffer Relay boards may be inserted in the Digital Termination Assembly. Each board contains 8 output digital input circuits. Therefore, two boards may be selected for each Sense Line Module. The actual boards implemented, and their location in a system, are shown on the System Configuration drawing. This drawing also specifies the screw termination designation for each digital input signal from the process.

BASIC OPERATION

As previously described, the Small System Digital Inputs hardware permits the system program to determine the status of 16 external digital inputs from switch positions, relay contacts, digital logic levels, etc. The status of the 16 inputs are read into memory by executing two consecutive Read Data instructions. The Small System Digital Inputs hardware provides the control to automatically read the upper 8-bit byte when the first Read Data instruction is executed and read the lower 8-bit byte when the second Read Data instruction is executed.

```
RDR1, LOC       Gates Byte 0 to LOC
RDR1, LOC+1     Gates Byte 1 to LOC+1
```

R1 is assumed to contain the device address.

The Digital input hardware control logic is reset by a single Output Command. Resetting the control logic ensures that the next Read Data instruction will read the status of the upper digital input byte (byte-0).

```
OCR1, X'10'
```

The Small System Digital Inputs hardware also provides an external interrupt line that may be momentarily enabled by the customer to inform the program that the inputs should be read. The interrupt may be armed and disarmed under program control by executing an Out Command instruction as shown below:

```
OCR1, X'80'     Disables interrupt

OCR1, X'40'     Enables interrupt
```

NUMBERED PINS*	LETTERED PINS*	LEVEL	HEXA-DECIMAL WEIGHT	SIGNAL	EXAMPLES OF DEVICE ADDRESSING		
					X'4C'	X'2B'	X'11'
0	A B	1 0	8	DAL00	0 To B	0 To B	0 To B
1	C D	1 0	4	DAL01	1 To C	1 To D	1 To D
2	E F	1 0	2	DAL02	2 To F	2 To E	2 To F
3	G H	1 0	1	DAL03	3 To H	3 To H	3 To G
4	J K	1 0	8	DAL04	4 To J	4 To J	4 To K
5	L M	1 0	4	DAL05	5 To L	5 To M	5 To M
6	N P	1 0	2	DAL06	6 To P	6 To N	6 To P
7	R S	1 0	1	DAL07	7 To S	7 To R	7 To R

*Located at position 20 on the Sense Line Module mother board.

Table 1 Address Selection

MNEMONIC	MEANING	FUNCTIONAL SCHEMATIC LOCATION
AD	Signal from the Address flip-flop	1R2
ADR	Address Pulse from Processor	3A1
ATN	Attention to the Processor	3A7
ATSYN	Attention Synchronization	3K5
B	Signal at S Input to Address flip-flop	1R1
BSATN	A High going pulse from the User that Sets the Interrupt Queue flip-flop	3R4
CMD	Command Pulse from Processor	3A2
CMG	Command Gated with Device Address	3112
DAL000 through DRL070	Data Available Lines	1A1 through 1A7
DR	Read Instruction From the Processor (RD)	3A4
DRG	DR, 0 Gated with the Device Address	3H4
DRL00 through DRL07	Data Request Lines	2C2 through 2C7
EBL	Enables the Interrupt When Low	3P1
GHIGH	Gate High Byte to Processor	4M7
GLOW	Gate Low Byte to Processor	4M6
RACK	Receive Acknowledge	3A8
SCLR	System Clear Signal	1A8
SR	Status Request from Processor	3A3
SRG	Status Request Gated with Device Address	3H3
SYN	Synchronization to Processor	3A5
TACK	Transmit Acknowledge	3A9

Table 2 Sense Line Module Mnemonic Dictionary

An external busy line input connection is also provided by the Small System Digital Inputs hardware that may be used to inform the system program when the digital inputs are ready to be monitored. Execution of the Sense Status instruction places the condition of the external busy line in the Busy Bit (bit 4) of the Status Byte.

SSR1, LOC

A summary of the Status and Command bytes is shown in Fig. 2.

The detailed operation of the digital input system during the execution of each of these commands is described in the following paragraphs. Most of this discussion is written for use with the Functional Schematic for the Sense Line Module. A dictionary of the mnemonics used in this Functional Schematic is provided in Table 2. Understanding the meaning of these mnemonics will be of assistance in understanding the operation of the digital inputs system.

Multiplexer Bus Interface

As previously described, the Small System Digital Inputs hardware communicates with the processor via the Multiplexer Bus. The Sense Line Module printed wiring board may be inserted into any available card slot in the Multiplexer Bus. The Digital Inputs hardware responds to the Multiplexer Bus control signals generated as the result of the execution of Output Command (OC) instructions, Read Data (RD) instructions, Sense Status instructions, Acknowledge Interrupt instructions, or the Initialize function.

The Multiplexer Bus Interface lines used by the Digital Inputs hardware are seen in Table 3.

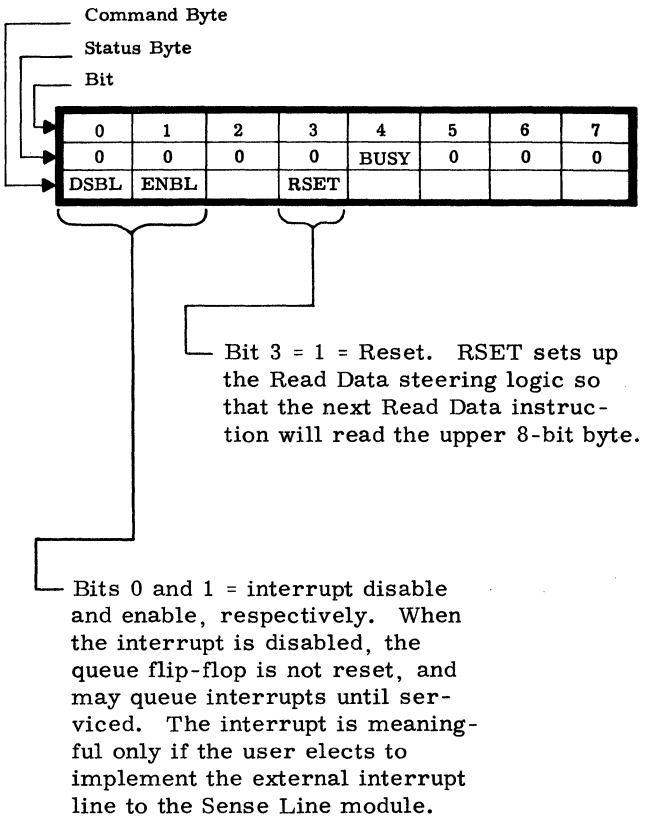

Fig. 2 Digital Input Status And Command Bytes

These signals are connected to the Sense Line Module mother board by the Field 0 connector. These signals are at 0 volts (±.5V) for true at the input of the Sense Line Module. Pin numbers associated with these connections are shown on sheet 5 of the Sense Line Module functional schematic.

Function	Mnemonic	Direction
Data Available Lines	*DAL00:07	Processor → Sense Line Module
Address Signal	ADRS	→
Data Available Pulse	DA	→
Command Pulse (OUT)	CMD	→
Status Request	SR0	→
Read Instructions	DR0	→
Data Request Line	*DRL00:07	←
Synchronized	SYNC	←
Attention	ATN	←
Transmit Acknowledge	TACK	To next controller on bus
Receive Acknowledge	RACK	→
Initialize	SCLR	→

*In a 3010/2 System, these signals are labeled D080;150

Table 3

Device Addressing

Each instruction executed to control the digital inputs hardware must address the Sense Line Module. The Sense Line Module address is normally X'11'. This address, however, may be changed by rearranging the jumper wires on the Sense Line Module mother board as described in the Options portion of this description. The following description applies to each instruction associated with the digital inputs hardware.

When the instruction is executed, the processor gates the address of the Sense Line Module on the Data Available Line (DAL00 thru DAL07 or D08 thru D15 in 3010/2 systems). The correct address presents all high inputs to the Address NAND gate as shown on sheet 1, coordinates L3 (1L3) of the Sense Module functional schematic. The Address NAND gate is enabled and its low output inverted to present a high B pulse at the S input of the Address flip-flop shown on 1P2.

The ADRS0 pulse from the processor is inverted (3D1) producing ADRS1. ADRS1 in conjunction with the B pulse, enables the NAND gates at 3F1 and 3D6, generating the Synchronizing signal (SYN0) back to the processor. The ADRS1 signal is also applied to the trigger input of the Address flip-flop at 1P2, and in conjunction with the high B pulse, sets the flip-flop. Setting the Address flip-flop generates the AD1 pulse. This AD1 pulse is then used to enable the functions associated with the instruction being executed.

Reset Control Logic

Executing an Output Command with bit 3 set (OC X'10') resets the Sense Line Module control flip-flop so that the next Read Data instruction will read the upper 8-bit byte (i.e., the inputs associated with S00 thru S07) of digital inputs.

During execution of the OC command with bit 3 set, the processor enables the DAL030 (1B4) and CMD0 (3A2) Control Lines. The CMD0 pulse, in conjunction with the AD1 pulse, generates the Synchronization pulse, SYN0 (3A6), back to the processor. The CMD pulse and the DAL03 pulse enable the DC clear input to the flip-flop at 4F7. In this manner, the flip-flop is reset. With the flip-flop at 4F7 reset, the next Read Data instruction executed will gate the status of the upper 8-bit byte of digital inputs to the processor. Fig. 3 illustrates the basic timing and control associated with the Output Command X'10' executed to the Digital Input hardware.

Read Data

Executing two consecutive Read Data instructions gates the status of the 16 digital input points into the processor. Each Read Data instruction reads one 8-bit byte of data from the digital inputs. The first Read Data instruction following an OC X'10' instruc-

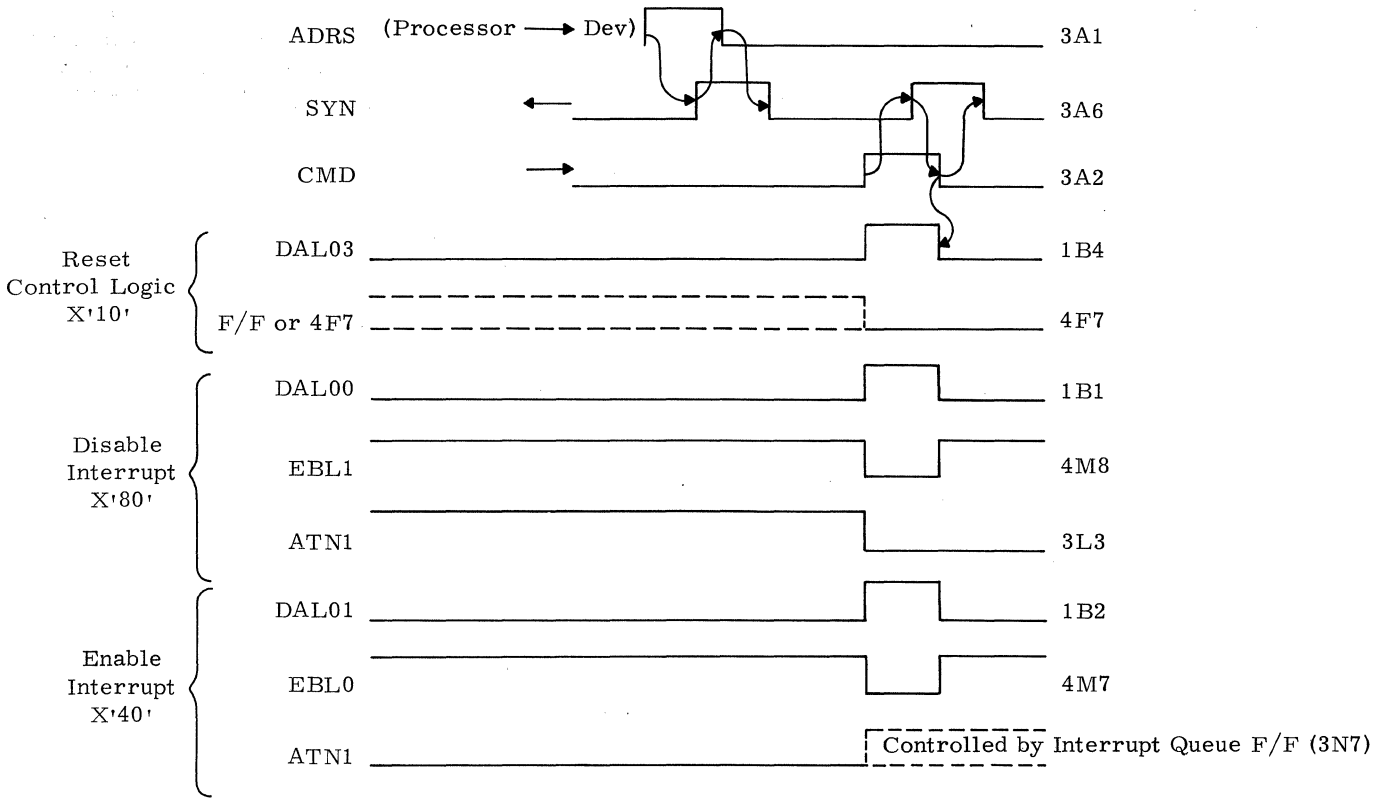

Fig. 3 Output Command Timing

tion or initialize, reads the upper byte (i.e., the inputs associated with S00 thru S07). The second Read Data instruction reads the lower 8-bit byte.

Fig. 4 illustrates the basic timing and control associated with Read Data instructions executed to the Digital Input hardware.

Executing the first Read Data instruction applies a DR0 pulse to the Sense Line Module (3A4). This signal, in conjunction with the AD1 pulse, enables DRG0 generating the Synchronization pulse, SYN0 (3A6), back to the processor. DRG is also applied to the trigger input of the flip-flop at 4F7 and to the NAND gates at 4H7. Assuming the flip-flop at 4F7 is reset from a previous OC X'10' instruction, signal GHIGH will be enabled. The trailing edge of the DRG pulse will set the flip-flop at 4F7 in preparation for the next Read Data instruction.

The GHIGH signal is applied to one input of the NAND gates associated with digital input points S00 thru S07 (byte 0). These gates are located at 4A3 thru 4G3 on the functional schematic. The digital inputs (high, +5V, for true) are connected to the other input of the NAND gates. In this manner, the status of the digital inputs are gated to the processor via the Data Request Lines (DRL) shown on sheet 2. Fig. 5 illustrates the flow of data from the digital input connections at the terminations thru the Sense Line Module to the processor.

During execution of the second Read Data instruction addressed to the digital inputs module, the flip-flop at 4F7 is set. The DR0 pulse from the processor again enables DRG. Because the flip-flop at 4F7 is set, the DRG pulse enables the GLOW pulse (4M7). The trailing edge of GLOW toggles the flip-flop at 4F7 to clear. The GLOW pulse is also applied to one input of the NAND gates associated with digital input points S08 thru S15 (byte 1). These gates are located at 4H3 thru 4P3 on the functional schematic. The digital inputs (high, +5V, for true) are connected to the other input of the NAND gates. In this manner, the status of the digital inputs are gated to the processor via the Data Request Lines (DRL) shown on sheet 2. Fig. 5 illustrates the flow of data from the digital input connections at the terminations thru the Sense Line Module to the processor.

Sense Status (Busy)

An external busy line may be connected to the Sense Line Module to inform the processor when the digital inputs are ready to be monitored. Executing a Sense Status instruction monitors this busy line. A busy indication will result in bit 4 of the Status Byte being set. A "ready to read" input will result in bit 4 being reset following the execution of the Sense Status instruction.

Fig. 5 illustrates the basic timing and functions performed in the Digital Inputs hardware by the Sense

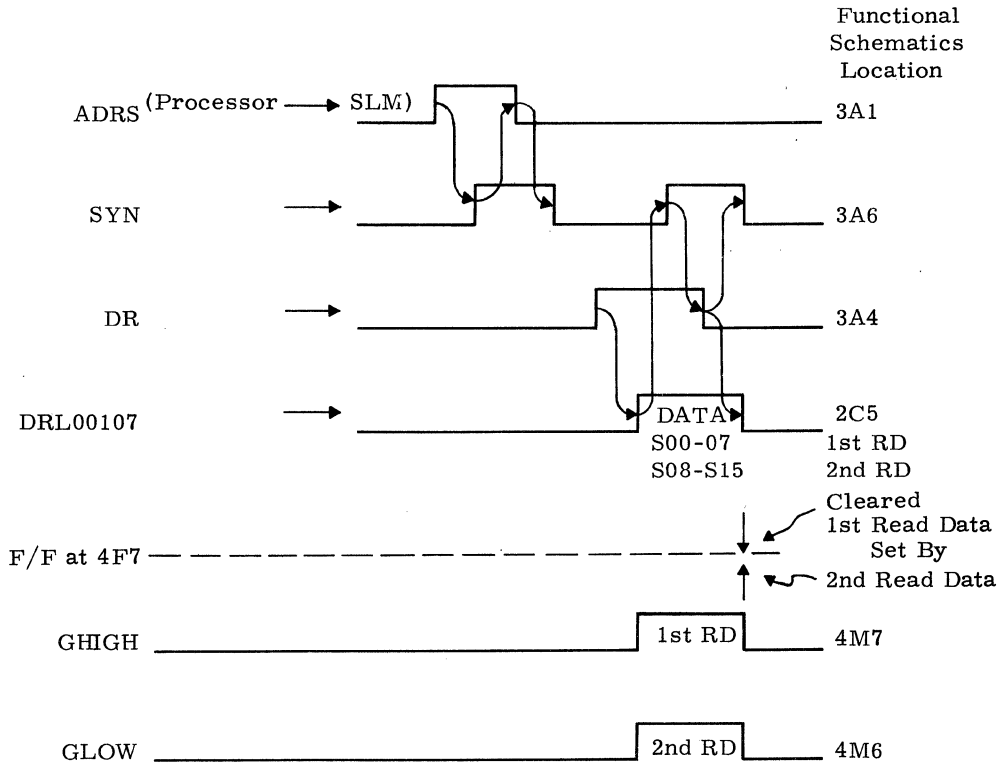

Fig. 4 Read Data Instruction Timing

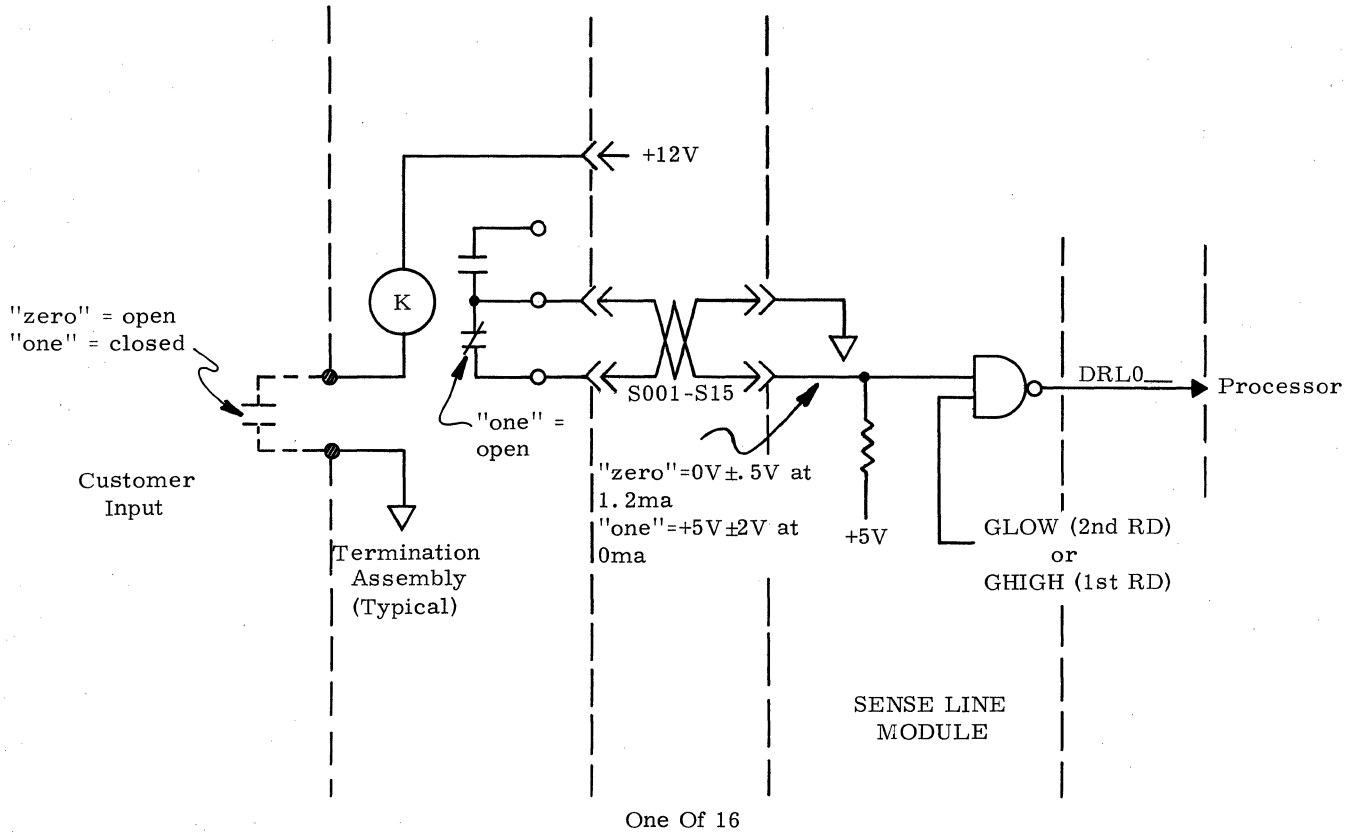

Fig. 5 Digital Input Circuit

Status instruction. During execution of the Sense Status instruction, the processor applies a Status Request signal, SR0, to the Sense Line Module (3A4). This SR0 signal, in conjunction with the address signal, AD1, generates SRG0, which enables the Synchronizing signal back to the processor. SRG0 is also applied to the NAND gate at 4N3. The NAND gate at 4N3 generates SRG1, which is applied to one input of the NAND gate at 4N5. The other input to the NAND gate at 4N5 is the Busy line from the customer. The busy line, when high (+5V), indicates a busy condition. When low, (0V), the line indicates the digital inputs are ready to be read. Therefore, when the busy line is high, a one is gated to the processor via the Data Request Line, DRL040, setting bit 4. When the busy line is low, bit 4 remains reset.

Interrupt Control

An external interrupt connection (BSATN1 on 3R9) to terminal 60-41 is provided on the Sense Line module. This permits a high going pulse from the customer input to enable an interrupt which may be used to initiate the system program to read the digital input points. This interrupt, when implemented, may be armed and disarmed by the system program. An OC X'40' enalbes the interrupt and an OC X'80' disables the interrupt.

Fig. 3 illustrates the basic timing and control functions associated with the execution of OC X'40' and OC X'80' instructions.

During execution of an OC X'80' instruction, the processor applies a CMD pulse and enables Data Available Line DAL00. These two signals are used to enable the NAND gate on 4K9, generating a low EBL1 pulse. This low EBL1 pulse resets the flip-flop on 3P2, generating a low ATN1 signal. This low ATN1 signal masks the output of the Interrupt Queue flip-flop, holding the Attention signal (ATN0) to the processor high. If the processor applies an acknowledge pulse (RACK0) in response to a different device interrupt, a TACK0 pulse will be generated (3B8) and daisy-chained to the next module on the bus.

During execution of an OC'40' instruction, the processor applies a CMD pulse and enables Data Available Line DAL01. These two signals are used to enable the NAND gate on 4K8, generating a low EBL0 pulse. This low EBL0 pulse sets the flip-flop on 3P2. Under this condition, the state of the Interrupt Queue flip-flop will control the attention (ATN) line to the processor. A positive going interrupt pulse on the BSATN1 input will generate a differentiated negative going pulse to set the Interrupt Queue flip-flop. Setting the Interrupt Queue flip-flop will generate a high ATN1 pulse which is inverted and applied to the processor to cause the program interrupt.

When the processor executes an Acknowledge Inter-

rupt instruction in response to the ATN1 signal from the digital input hardware, a RACK0 pulse is applied to the Sense Line Module on 3A8. This RACK pulse generates the ATSYN pulse which toggles the Interrupt Queue flip-flop to clear. The ATSYN0 pulse (3K6) enables the Address Line inputs (1C8) which enables the device address selected by the jumper wiring to one input of the NAND gates at 2M5. The other input of the NAND gate (ATSYN1) is also enabled which gates the device address to the processor, via the Data Request Lines.

Initialize

Pressing the INITialize switch on the console applies a SCLR0 pulse to the Sense Line Module on 1A8. This SCLR0 pulse resets the Address flip-flop at 1P2, resets the flip-flop at 4F7, resets the Interrupt Queue flip-flop at 3N7, and disables interrupts by resetting the flip-flop at 3P2. In this manner, the Sense Line Module control logic is initialized.

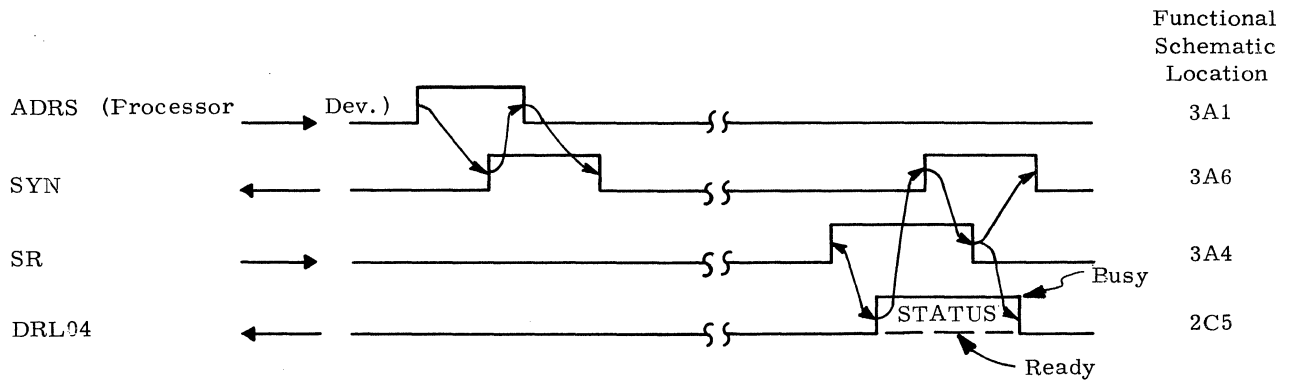

Fig. 6 Sense Status Instruction Timing