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UNIVERSAL CLOCK INSTRUCTION MANUAL

Consists of:

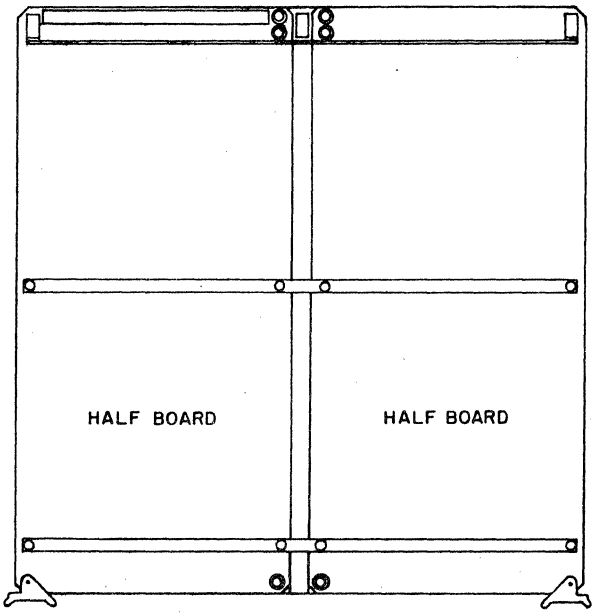
Installation Specification	02-240A20
Maintenance Specification	02-240R02A21
Programming Specification	02-240R01A22
Schematic	02-240R01D08

INTERDATA®
2 CRESCENT PLACE, OCEANPORT, NEW JERSEY 07757 | (201) 229-4040

UNIVERSAL CLOCK INSTALLATION SPECIFICATION

1. INTRODUCTION

This specification provides the necessary information for the installation of the 02-240 Universal Clock Module and the external clock option. The module assembly consists of one standard 35-398 half board and one 17-177 cable. The 35-398 half board must be strapped to a blank half board (INTERDATA 16-398 Half Board Kit) or an active half board (i.e. Memory Protect) to be installed in a chassis designed for full boards. The Universal Clock board may be used in either the right or left half position, as required. See Figure 1.



NOTE: 35-398 HALF BOARD CAN BE LOCATED ON EITHER SIDE.

Figure 1. Half-Board Assembly

2. INSTALLATION

2.1

When the Universal Clock Module is shipped with a system, it is installed at the factory so there is no special unpacking procedure. It is only necessary to insure that the module is properly seated in its connectors. If the module assembly is purchased separately, it should be unpacked carefully and inspected for damage prior to installation.

2.2 Location

The 35-398 Universal Clock Module half board, strapped to a blank or active half board, may be installed in any I/O slot. However, it is preferable to use the highest priority position available. After installing the module, remove the RACK0/TACK0 strap located on the back panel between Terminals 222 and 122 of the selected slot.

2.3 Cables and Connectors

Connect the 17-177 cable as shown in Figure 2. Note that the cable is long enough to allow the 35-398 half board to operate on an extender.

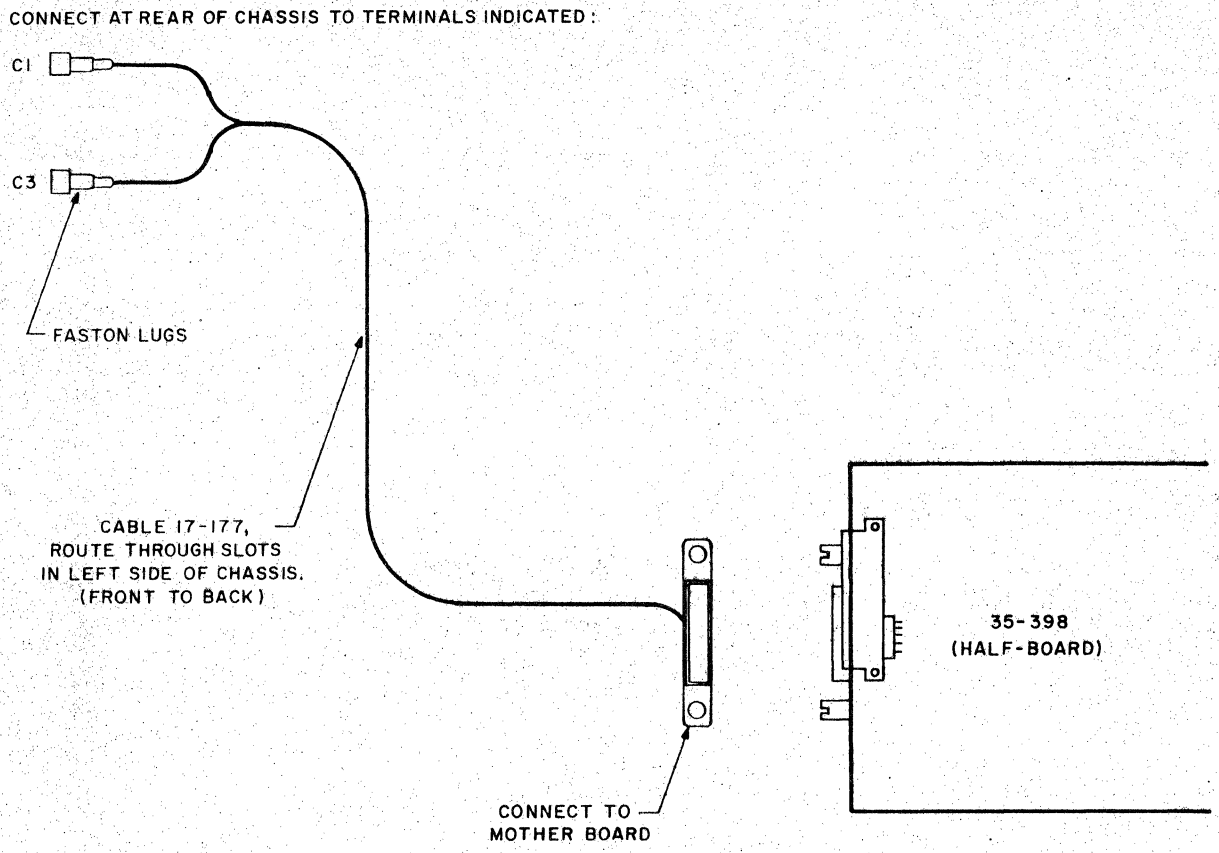


Figure 2. Cable Connections

3. EXTERNAL CLOCK OPTION

To use an external time base oscillator perform the following steps: (Refer to Schematics 02-240D08)

1. Strap Test Point (TP) A to Test Point (TP) B.
2. Connect the external oscillator, via twisted pair, to Test Point EXT and Test Point EXG (TP EXG is ground).

Internal termination of the Universal Clock Module is shown in Figure 3.

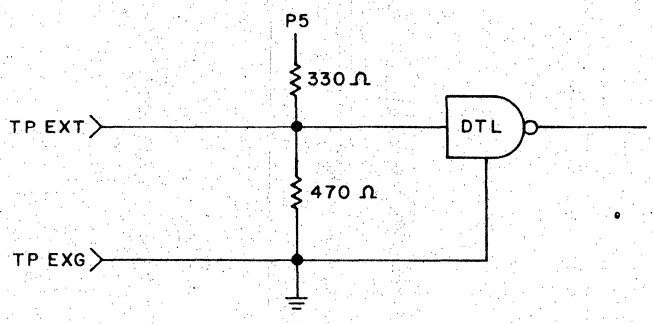


Figure 3. External Oscillator Connections, and Internal Termination

UNIVERSAL CLOCK MAINTENANCE SPECIFICATION

1. INTRODUCTION

The 02-240 Universal Clock Module consists of two I/O devices; 1. the programmable Precision Interval Clock (PIC), and 2. the AC Line Frequency derived Clock (LFC). The PIC provides the user with a Processor interrupt and a program accessible counter which is based on a dynamically variable (thru program control) Precision Resolution Clock and Interval Counter. The LFC is derived from the AC power line and provides the user with a Processor interrupt at twice the line frequency.

Since the PIC and LFC are completely independent of each other, they are covered in separate sections of this specification. Section 2 describes the PIC, and Section 3 describes the LFC. Both sections contain block diagram and functional schematic analysis, timing information, and sufficient notes to maintain this interface. A mnemonic list common to both sections is provided at the end of this specification.

2. PRECISION INTERVAL CLOCK

2.1 Block Diagram Analysis

As shown in the PIC block diagram on Sheet 4 of Schematic 02-240D08, the Count Input Buffer and Resolution Select input Buffer are loaded from the Multiplexor Bus. Upon initial start up or at the end of an Interval period, this information is transferred to the Interval Counter and Resolution Select Register. The Resolution Select Register enables one of the four Resolution Clock rates available from the Clock Divider. The selected Clock Divider output Count Pulse (COUNT0) decrements the Interval Counter until it reaches zero, the next count pulse produces the PIC Interrupt (XNT1) which is sent to the attention circuits, and the process is repeated. The Interval Counter may be monitored through the Counter Output Buffer to the Multiplexor Bus.

2.2 Functional Diagram Analysis

Refer to Functional Schematic 02-240D08 for the following analysis.

With the exception of common I/O bus buffering, the PIC logic is detached from the LFC. Status, Command, and Data Byte information is provided in the Programming Specification 02-240A22.

2.2.1 Operation. Initialization (SCLR0)(1L8) insures that the PIC is placed in the Disarm Mode by resetting the Enable PIC Interrupt (ENAX1)(1J1) and PIC Disarm (XDRM0)(1J2) flip-flops. The Resolution and Counter Input Buffers (2C1-9), and the Overflow (OVFL)(2H2), Data Byte Count (DBC1)(2H8), and Write Byte (WBC0)2H3) flip-flops are cleared.

The Resolution and Interval data is initially loaded into the PIC's Input Buffers (2E1-9) in two data bytes by Load Data Low (LDL0)(2M6) and Load Data High (LDH0)(2M7). A Start Command (CMGX0·DAL21) momentarily sets the START1 flip-flop (1J8), the next Raw Clock pulse resets it (RCLK0)(1H8). This action resets the PIC Interrupt flip-flop (XNT0) (2G7), and loads the Resolution Select Register (2E1-2) and the Interval Counter (2E3-9) from the Input Buffers. XANT1 (3J2) goes active if enabled.

The Resolution Register outputs (SMS1, SHMS1, STMS1, and SCK1) enable one of the Clock Divider outputs (3D1-9) to produce COUNT0 (3M7). COUNT0 starts to decrement the Interval Counter. When zero, the next count pulse activates the borrow output from the Interval Counter (2E3-9) and the XNT1 flip-flop (2G7) momentarily sets, it is reset by CLK1. This causes an interrupt to be queued in the PIC Attention flip-flop (XANT1)(3J1) if not in the Disarm Mode. Attention goes active (ATN0)(3N1), if enabled. The XNT0 pulse reloads the Resolution Select and Interval Counter Registers from the Input Buffers. Operation now proceeds as previously described.

During the Interval (Interval Counter has not reached zero), the Input Buffers may be altered by two data bytes containing a new Resolution and/or Interval. When the present Interval concludes, the new data will be loaded from the Input Buffer in place of the old. However, if the Interval times out between the start of the first data byte transferred and the end of the second data byte transferred, the Write Byte Count flip-flop (WBC)(2H3) causes the Overflow flip-flop to set (OVFL)(2H2). This stops the Clock by holding START0 low (1J7). The clock will restart after the completion of the second data byte transfer or on receipt of a Start Command. OVFL remains set until the execution of a Sense Status, an Acknowledge Interrupt instruction, or Initialization.

The PIC is provided with an Output Buffer (3G1-9) so that the Interval Counter may be interrogated without disturbing its operation, by using two data byte transfers. The Output Buffer is normally loaded on every CLK1. The first Data Request gated (DRG0)(1R4) by Raw Clock (RCLK1)(1J9) latches up the Output Buffer by setting the Data Request Sync flip-flop (DRSYN1)(2J7), which in turn holds Load Buffered Count high (LDBC0)(2K7). The Read Data Low (RDL0)(2L6) is activated and SYN0 is returned. The falling edge of DRG1 sets the Read Byte Counter. The second DRG1 activates Read Data High (RDH0)(2L7) and SYN0 is returned. The falling edge of the second DRG1 resets the Read Byte Counter, which in turn resets the DRSYN1 flip-flop.

2.2.2 Circuit Analysis. It should be noted that numerous 19-035 four bit up-down counters are used as registers and perform no counting operations. The One-Shot (3R6) which resets the PIC Attention flip-flop (XATN1)(3J1) is set to produce a 175 nanosecond pulse (approximately).

2.3 Timing

Refer to Figure 1.

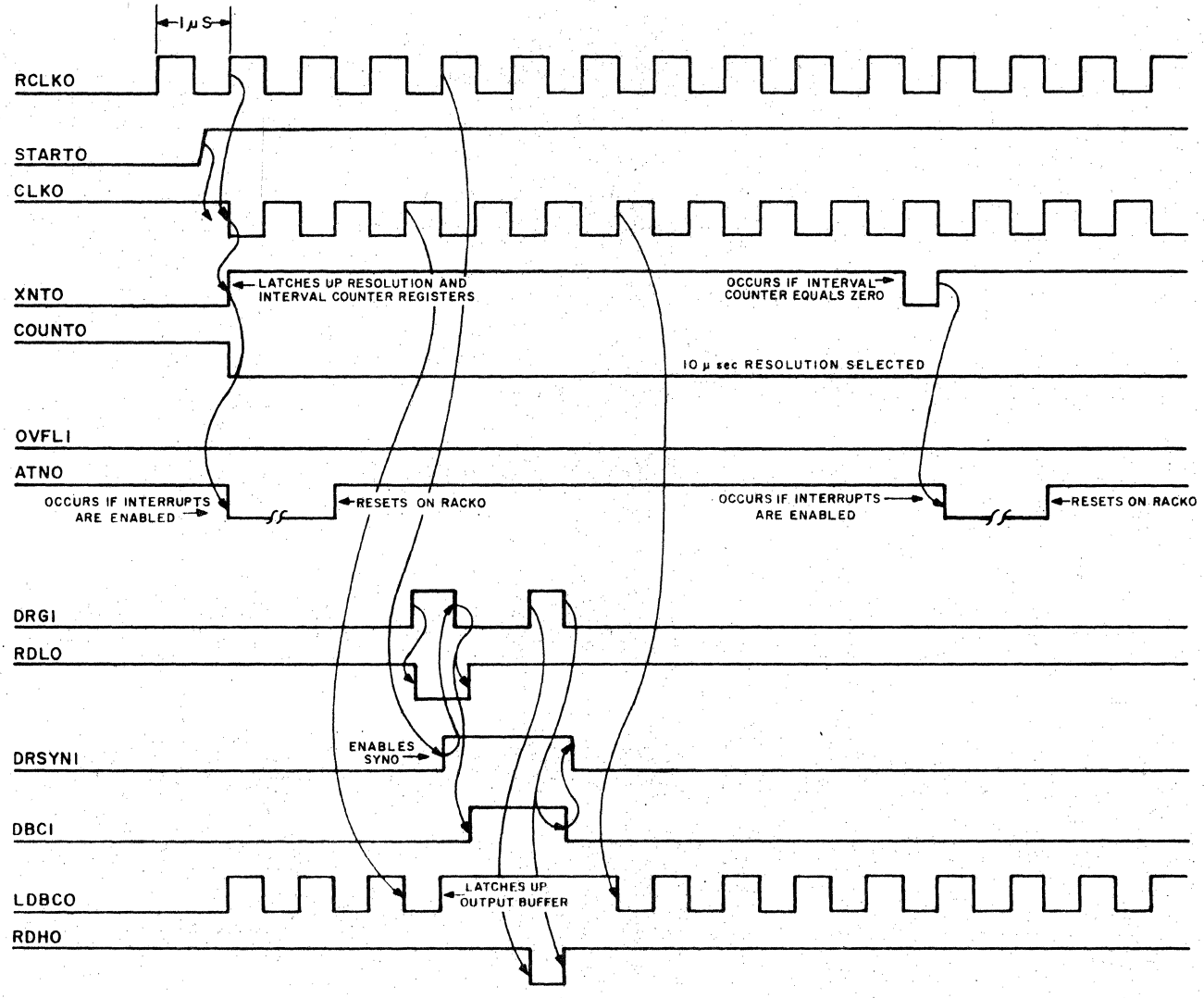


Figure 1. Precision Interval Clock Timing Diagram

2.4 Routine Maintenance, Adjustments, and Tests

The PIC requires no adjustments. The accuracy of the crystal oscillator should be checked with a digital frequency meter on RCLK0 (1J9) at Test Point Z (1MHZ ± .01%).

2.5 Troubleshooting

The PIC may be reasonably tested using a static check. Refer to the Programming Specification, 02-240A22, for set up procedures. Test Program 06-123 provides a dynamic check which can be monitored by appropriate test equipment.

3. LINE FREQUENCY CLOCK

3.1 Block Diagram Analysis

As shown in the LFC block diagram (Figure 2), the power supply provides a 12 VAC line from which the LFC Interrupt (HNT1)(3R8) is derived. Although shown separately for clarity, the LFC I/O logic (Address, Command and ATN circuits) is combined with that of the PIC. This is described in Section 4.

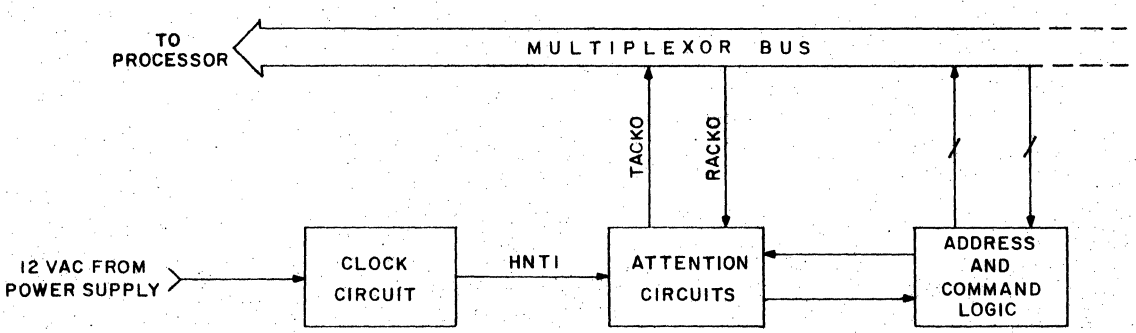


Figure 2. AC Line Derived Clock Block Diagram

3.2 Functional Diagram Analysis

As shown on Sheet 3 of Functional Schematic 02-240D08, the clock circuit is driven by the 12 VAC output from the system power supply. A full wave bridge rectifier, followed by a zero voltage detector whose output is fed through two gates, produces the HNT1 pulse (3R8) at twice the line frequency. The LFC is placed in the Disarm Mode by SCLR0, resetting the Enable LFC Interrupt (ENAH1)(1J5) and the LFC Disarm (HDSRM0)(1J5) flip-flops. The LFC responds only to the Enable and Disable Commands. If the LFC is not in the Disarm Mode, HNT1 will toggle the LFC Attention flip-flop set (HATN1)(3K6) at twice the line frequency. Attention (ATN0)(3N1) is activated, if enabled.

4. PIC AND LFC I/O FUNCTIONAL ANALYSIS

The Addresses of the PIC and LFC differ only by the state of Bit-7. The PIC address is always even (Bit-7 inactive), while the LFC address is always odd (Bit-7 active). The output of the PIC Address flip-flop (ADX1)(1J4) and LFC Address flip-flop (ADH1)(1J4) gates the control lines (DR0, DA0, SR0, and CMD0) to their respective logic.

The interrupt logic (Sheet 3) is arranged so that the PIC has the highest interrupt priority. Reference should be made the Model 70 User's Manual, Publication Number 29-261, for a description of standard I/O timing sequences. Refer to the Programming Specification, 02-240A22, for Command, Status, and Data Byte information.

5. MNEMONICS

The following list provides a brief description of each mnemonic found in the Universal Clock. The source of each signal on the Schematic Drawing, 02-240D08, is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
AD	Address - Bit-7 of device address returned on SRG.	3S4
ADH	Address LFC - Active when the LFC address is recognized.	1J4
ADR	Address - Decoded address.	1G3
ADRS	Address - The Processor presents an Address Byte on Data Lines D08:15. The device controller accepts the Address Byte and responds with a SYN.	1K1
ADX	Address PIC - Active when the PIC address is recognized.	1J4
AG001:061	Address Gate Lines - Selected straps which generate a unique device address.	1F2-8
ATN (Test Point U)	Attention - Any device desiring to interrupt the Processor will activate the ATN line and hold this line until an ACK is received from the Processor.	3N1
ATSYN	Attention Synchronize - Strobes the address of the interrupting device to the Processor.	3S4
BCT00-11	Buffered Count Output - Output lines of Output Buffer.	3H2-8
CLK	Clock - Raw Clock gated.	1L9
CMD	Command - The Processor presents a Command Byte on Data Lines D08:15. The device controller accepts the Command Byte and responds with a SYN.	1K2
CMGH	Command Gated for LFC - Command gated by ADH.	1R5
CMGX	Command Gated for PIC - Command gated by ADX.	1R2
CNT00-11	Counter Output - Output lines from Interval Counter.	2F3-8
COUNT (Test Point S)	Count - Count pulse at selected Resolution Rate.	3M7
D080:150	Data Lines - Data Lines D080:150 are used to transfer one eight bit byte of data between the Processor and the device. One byte of address or command is transferred from the Processor to the device over Data Lines 8:15 (D08:15) when accompanied by either an Address (ADRS) or a Command (CMD) control line. One byte of data is transferred from the Processor to the device when accompanied by the Data Available (DA) control line. The device, in response to an Acknowledge (ACK) control line or a Sense Status (SR) control line, sends one byte of address or status information to the Processor over Data Lines D08:15. In response to a Data Request (DR) control line, the device sends an eight bit byte of data to the Processor. The device always sends a Synchronize (SYN) signal to the Processor to indicate that it has either received the data from the Processor or that it has sent the data to the Processor. The SYN signal is removed immediately after the Processor removes the control line.	1A2-8

MNEMONIC	MEANING	SCHEMATIC LOCATION
DA	Data Available - The Processor presents data on Data Lines D080:150 for transfer to the device. The device controller accepts the low byte and responds with a SYN.	1K3
DAG	Data Available Gated - Data Available gated by ADX.	1R3
DAL00:70 01:71	Data Available Lines - Data Lines D080:150 buffered double rail for data transfer to the device.	1D2-8
DBC	Data Byte Count - Toggles on DAG or DRG.	2J8
DR	Data Request - The device controller presents data to Data Lines 8:15 followed by a SYN.	1K4
DRG	Data Request Gated - Data Request gated by ADX.	1R4
DRSYN	Data Request SYN - Enables SYN on DRG.	2J7
ENAH	Enable LFC Interrupt - Gates HATN to ATN.	1J5
ENAX	Enable PIC Interrupt - Gates XATN to ATN.	1J1
EXC	External Clock - External time base oscillator connection.	1H9
EXG	External Ground - Ground for EXC.	1H9
HATN	LFC Attention - Queue flip-flop for LFC Interrupt.	3K6
HDSRM	LFC Disarm - Holds HATN reset, when active.	1J5
HMS	100 microseconds - Clock Divider output for 100 microseconds.	3D6
HNT (Test Point V)	LFC Interrupt - Pulsed at twice line frequency.	3S8
LDBC	Load Buffered Count - Loads Output Buffer.	2K7
LDH	Load Data High - Loads high byte of Input Buffer	2L7
LDL	Load Data Low - Loads low byte of Input Buffer	2L7
MS	1 millisecond - Clock Divider output for one millisecond.	3D8
OVFL (Test Point R)	Overflow - Set on XNT· DBC	2H2
RACK	Receive Acknowledge - Control line activated by the Processor in response to an interrupt.	3G4
RCLK (Test Point Z)	Raw Clock - Buffered output of internal or external time base oscillator.	1J9
RDH	Read Data High - Enables High Byte from Output Buffer to data lines.	2L7
RDL	Read Data Low - Enables Low Byte from Output Buffer to data lines.	2L6
SCLK	Select Clock - Enable Clock Divider output for one microsecond.	2F1

MNEMONIC	MEANING	SCHEMATIC LOCATION
SCLR	System Clear - This is a metallic contact to ground that occurs during Power Fail, Power Up, or Initialize.	1L8
SHMS	Select 100 microseconds - Enable Clock Divider output for 100 microseconds.	2F1
SMS	Select one millisecond - Enable Clock Divider output for one millisecond.	2F1
SR	Status Request - The device controller must present device status to Data Lines D08:15 followed by a SYN.	1K3
SRG	Status Request Gated - Status Request gated by ADX.	1R4
SSTRT	Set Start - Sets Start flip-flop.	2K1
START	Start - Start Clock. Enables CLK1.	1K8
STMS	Select 10 microseconds - Enable Clock Divider output for 10 microseconds.	2F1
SYN	Synchronize - This signal is generated by the device to inform the Processor that it has properly responded to a control line.	1S1
TACK	Transmit Acknowledge - System daisy chain control line to the I/O system.	3S3
TMS	10 microseconds - Clock Divider output for 10 microseconds.	3D4
WBC	Write Byte Count - Toggles on DAG only.	2H4
XATN	PIC Attention - Queue flip-flop for PIC interrupt.	3J1
XDSRM	PIC Disarm - Holds XATN reset when active.	1J2
XNT (Test Point T)	PIC Interrupt - Pulsed on completion of Interval Count.	2G6
XRP	1Kohm Resistor to Pt(+5).	2F9

UNIVERSAL CLOCK PROGRAMMING SPECIFICATION

1. INTRODUCTION

The Universal Clock Module consists of two I/O devices; the programmable Precision Interval Clock (PIC), and the AC Line Frequency derived Clock (LFC). Since the PIC and LFC are completely independent of each other, they are covered in separate sections of this specification. Section 2 describes the PIC, and Section 3 describes the LFC.

2. PRECISION INTERVAL CLOCK

2.1 Description

The PIC provides the user with a Processor interrupt and a program-accessible counter which is based on a dynamically variable (thru program control) Precision Resolution Clock generator and Interval Counter.

As shown in Figure 1, PIC block diagram, the master time base for the PIC is provided by a one megahertz crystal oscillator. It should be noted that the internal oscillator can be disabled so that an external master time base oscillator may be used. See Installation Specification 02-240A10, for details.

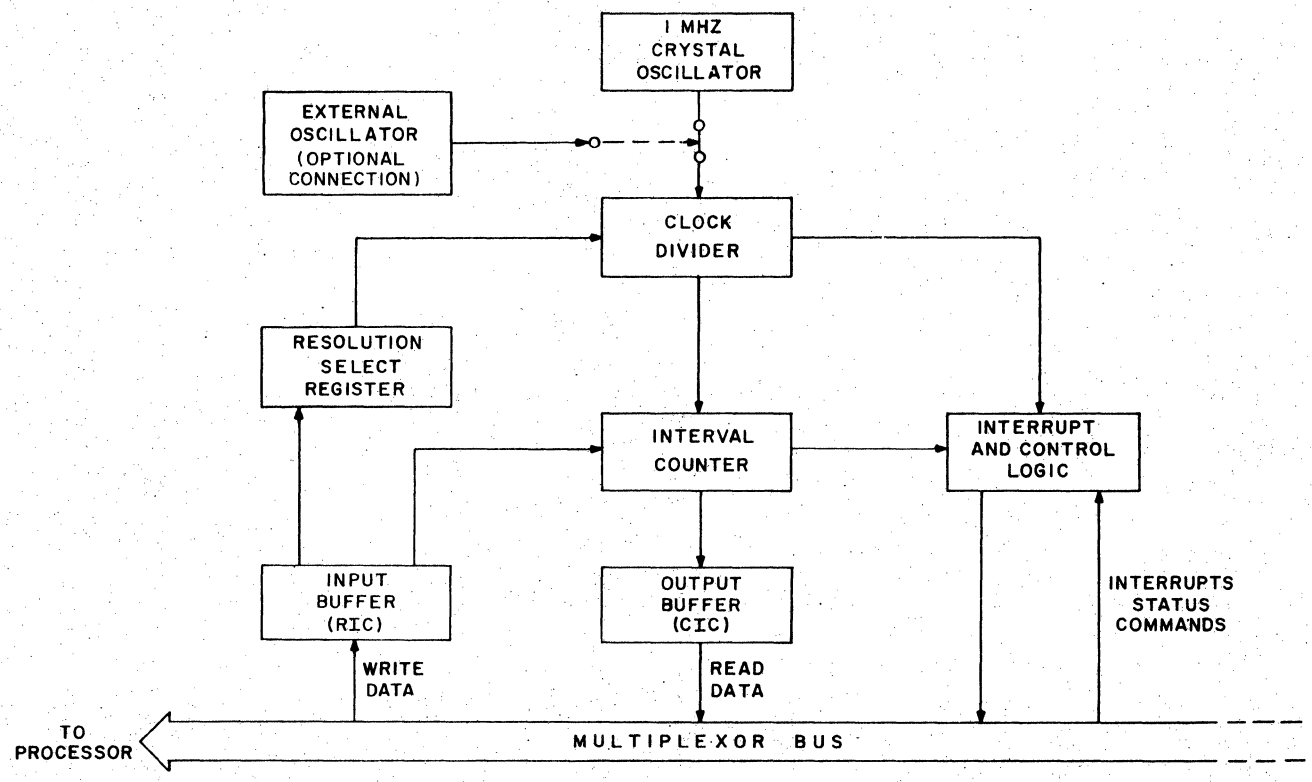


Figure 1. PIC Block Diagram

2.2 Operation

The basic PIC operation is:

1. The Resolution and Interval data is sent to the PIC by Write Data or Write Halfword instructions, and it remains in the Input Buffers until new data is supplied.

2. When the clock is started by an Output Command, the Resolution and Interval data in the Input Buffers is transferred to the Resolution Select Register and Interval Counter and an interrupt is generated if enabled. The Interval Counter begins to decrement at the selected resolution rate.

3. At the conclusion of the interval count (Interval Counter reaches zero) the next clock pulse causes the Interval Counter and Resolution Select Register to be reloaded from the Input Buffers. The clock continues to run and once again begins to decrement the Interval Counter.

4. The PIC generates an interrupt each time the Interval Counter and Resolution Select Register are reloaded from the Input Buffer if interrupts are enabled. Further, the PIC queues an interrupt if interrupts are disabled and not disarmed. Finally, the PIC neither generates nor queues an interrupt under the above circumstances if interrupts are disarmed.

5. The PIC is provided with an Output Buffer Register so that the Interval Counter may be interrogated at anytime without disturbing its operation. The contents of the Output Buffer does not change while it is being read by the Processor.

Note in Steps 2 and 3 that the Input Buffers are used by the PIC only at the beginning of each interval to reload the Resolution Select Register and Interval Counter. Hence, the Input Buffers are free to accept new data anytime during the remainder of the interval. Therefore, the user may output new Resolution and Interval data to the Input Buffers before the present interval concludes. When the present interval times out, the new data is loaded in place of the old and the PIC continues at the new Resolution and Interval.

If the present interval concludes during the time that the Input Buffers are being altered, an overflow condition exists causing the clock to pause until data transfer to the Input Buffers is completed or the PIC is issued a Command Start.

NOTE

Overflow only resets on the execution of Sense Status or Acknowledge Interrupt instructions, or on Initialization. If Overflow occurs and is not reset by one of the above, the new clock interval will not be accurate.

NOTE

If a zero is loaded, the clock duration equals the resolution.

Using the internal time base oscillator, the following resolutions and intervals may be obtained:

RESOLUTION	INTERVAL
1us	1us to 4,096us
10us	10us to 40,960us
100us	100us to 409,600us
1ms	1ms to 4,096ms

2.3 Program Instructions

Command, Status and Data bytes for the PIC are shown on Table 1.

2.4 Program Sequences

Write instructions (WD, WDR, WH, or WHR) are used to initially set up or change the Resolution and Interval Count (RIC). To change the RIC, data transfers must be completed within the present clock interval or overflow status (OVFL) results.

When the interval times out, and the Interval Counter is reloaded, an interrupt is generated, if enabled; queued if disabled; and not queued if disarmed. Also, the RIC is loaded into the Resolution Select Register and Interval Counter, and the clock continues to run.

Command Start (OC or OCR with Bit-2 in the Command Byte set) is used to initially start or to reload the RIC and restart the clock.

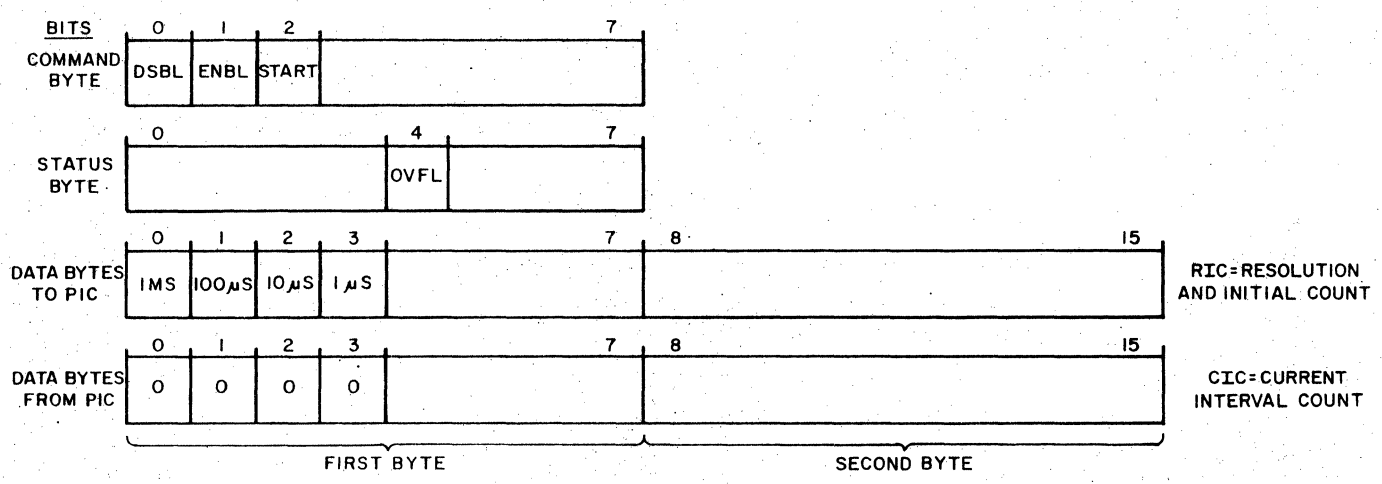
Read instructions (RD, RDR, RH, or RHR) are used to interrogate the Current Interval Counter (CIC) during the count period.

Typical procedure for the PIC is:

1. Output two data bytes using the Write instructions to select the clock period.
2. Disarm device interrupts and start the clock using a Command instruction.
3. Enable device interrupts using a Command instruction.
4. Monitor the Interval Counter, if appropriate, by inputting two data bytes using the Read instructions.
5. If necessary, output new data bytes to change the RIC. Status can be checked for overflow condition, which would indicate that the new clock interval was not started on time.
6. To stop the PIC, output two bytes to the RIC with all Resolution bits zero, and issue a Command Start.

The PIC interrupts at the conclusion of each clock interval when the Interval Counter is reloaded, if enabled. It should be noted that the clock normally does not stop but merely creates an interrupt and restarts using the last selected RIC. This interrupt should be serviced with an Acknowledge Interrupt instruction, an Immediate Interrupt, or an appropriate Channel Command Block.

TABLE I. PIC STATUS AND COMMAND BYTE CODING



COMMAND BYTE

DSBL	DISABLE INTERRUPT: Setting this bit prevents the device from interrupting the Processor, but allows interrupts to be queued.
ENBL	ENABLE INTERRUPTS: Setting this bit allows the device to interrupt the Processor.
DISARM	Setting both the DISABLE and the ENABLE bits prevents the device from interrupting or queuing the interrupts, and clears any queued interrupts.
START	Setting this bit stops the clock, reloads the Resolution Select Register and Initial Count from the Input Buffers, then restarts the clock.

NOTE

The PIC either generates or queues an interrupt each time a START command is issued unless that command also sets (or a previous command has set) the PIC to the Disarm Mode.

STATUS BYTE

OVFL — OVERFLOW: This bit is set if the interval times out during the time between the beginning of the first data byte transfer and the end of the second byte transfer to the device. If Overflow sets, counting stops. Counting resumes after a Command Start, or at the completion of the second data byte transfer. This bit resets on the execution of Sense Status or Acknowledge Interrupt instructions, or on Initialization.

DATA BYTES

Data Byte Transfers to PIC (Write). See Note 1.

First Data Byte	Bits 0:3 specify Resolution. See Note 2. Bits 4:7 specify the four most significant bits of the Interval Count.
Second Data Byte	Bits 0:7 specify the eight least significant bits of the Interval Count.

Data Byte Transfers from PIC (Read). See Note 1.

First Data Byte	Bits 0:3 return as zero. Bits 4:7 return the four most significant bits of the current Interval Count.
Second Data Byte	Bits 0:7 return the eight least significant bits of the current Interval Count.

Note 1. The byte pointer is reset upon Initialization or any command; otherwise, it toggles on any data transfer (Read or Write).

Note 2. If no Resolution bits are set, the count stops. If more than one Resolution bit is specified, the shortest Resolution is used.

2.6 Initialization

Initialization occurs on power up or when the Initialize button is depressed. After Initialization, the PIC is left in the Disarm Mode with the Resolution and OVFL bits reset.

2.7 Device Number

The INTERDATA preferred address is X'6C'. The PIC address must be even. Wire changes (see Maintenance Specification 02-240A21) can select any even number address for this device. See the sample program in Appendix 1.

3. AC LINE FREQUENCY DERIVED CLOCK

3.1 Description

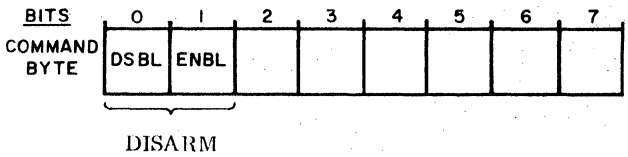
The LFC interrupt rate is derived from the AC power line. The clock rate is twice the line frequency.

POWER LINE FREQUENCY	CLOCK RATE
60Hz	8.33ms per interrupt
50Hz	10 ms per interrupt

3.2 Program Instructions

The Line Frequency Clock has only a Command Byte as shown in Table 2. All zero status is returned on any Sense Status instruction. Data transfer instructions have no effect on the device.

TABLE 2. LFC COMMAND BYTE CODING



DSBL	DISABLE INTERRUPT: Setting this bit prevents the device from interrupting the Processor, but allows interrupts to be queued.
ENBL	ENABLE INTERRUPTS: Setting this bit allows the device to interrupt the Processor.
DISARM	Setting both the DSBL and the ENBL bits prevents the device from interrupting or queuing the interrupts, and clears any queued interrupts.

3.3 Program Sequence

The LFC has no set up procedure other than to enable interrupts with an Output Command instruction (OC or OCR).

3.4 Interrupts

The Line Frequency Clock, if enabled, interrupts at twice the line frequency. This interrupt should be serviced with an Acknowledge Interrupt instruction, an Immediate Interrupt, or an appropriate Channel Command Block. A status of all zeros is returned with Sense Status or Acknowledge Interrupt instructions.

3.5 Initialization

The LFC is initialized on power up or by depressing the Initialize button. After Initialization, the LFC is placed in the Disarm Mode.

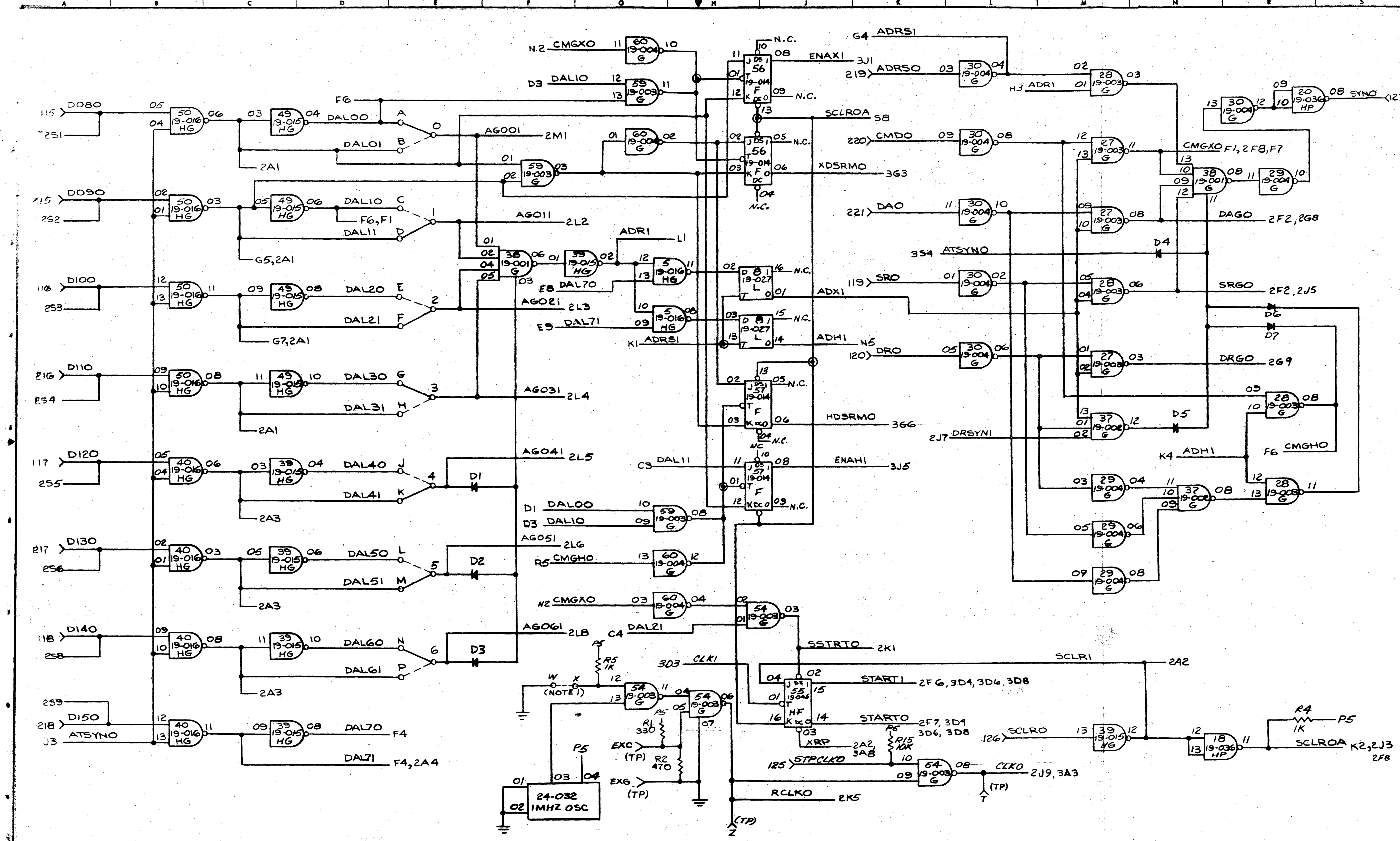
3.6 Device Number

The INTERDATA preferred address is X'6D'. The LFC address must be odd. The most significant address bits are always the same as for the PIC.

APPENDIX 1

```
*          PIC SAMPLE PROGRAM
*          THIS PROGRAM CAUSES THE PRECISION INTERVAL CLOCK
*          OF THE UNIVERSAL CLOCK MODULE TO CREATE A PROCESSOR
*          INTERRUPT EVERY 4MS AND 8MS SEQUENTIALLY WITH 1MS
*          RESOLUTION
*
DEVN       EQU   13
OVFL       EQU   14
R15        EQU   15
*
ORG        LHI   DEVN,X'6C'          LOAD DEVICE NUMBER
           LHI   R15,CLKINT          SET UP SERVICE PNTR TABLE
           STH   R15,X'D0'+X'D8'     FOR DEVICE NO. X'6C'
           WH    DEVN,FMS            SET RIC FOR 4 MS
           OC    DEVN,START
           WH    DEVN,EMS            SET RIC FOR 8 MS
           SSR   DEVN,OVFL
           BTC   8,ERROR
           LPSW  WAIT
ERROR      LPSW  HALT
WAIT       DC    X'C800',ORG
HALT       DC    X'8000',ORG
FMS        DC    X'8004'             1 MS RATE, 4 COUNTS
EMS        DC    X'8008'             1 MS RATE, 8 COUNTS
START      DC    X'6000'             ENABLE,START
*
*  INTERRUPT ROUTINE
*
SAVE       DS    6                   REGISTER SAVE AREA
CLKINT     DS    4                   OLD PSW STORED HERE
           DC    0                   NEW PSW STATUS
           STM   DEVN,SAVE           SAVE 3 REGISTERS
           LHI   DEVN,X'6C'
           RHR   DEVN,R15            READ CIC
           CLHI  R15,5               CIC < 5 MEANS
           BLS   NEXT8               CURRENT INTERVAL IS 4MS
           WH    DEVN,FMS            NEXT INTERVAL 4MS
           BS    TEST
NEXT8      WH    DEVN,EMS            NEXT INTERVAL 8MS
TEST       SSR   DEVN,OVFL           ERROR STOP ON OVFL STATUS
           BTC   8,ERROR
           LM    DEVN,SAVE           RESTORE REGISTER
           LPSW  CLKINT              EXIT INTERRUPT ROUTINE
           END
```

INTERDATA®



NOTES
1. STRAP TO GND TO USE EXTERNAL CLOCK.
2. STANDARD ADDRESS IS X'6C' OR '6D'.

REVISIONS				
SHT. 3 - ADDED R16 & C4				
			6-14-72	R01

NAME	TITLE	DATE
P. EDWARDS	DRAFT	10-6-71
G.J HOMEFIELD	CHK	11-19-71
R. MOHL	ENGR	1-10-72
D.W. YOUNG	SYS TST	1-10-72
RE JONES	DIR ENG	1-11-72

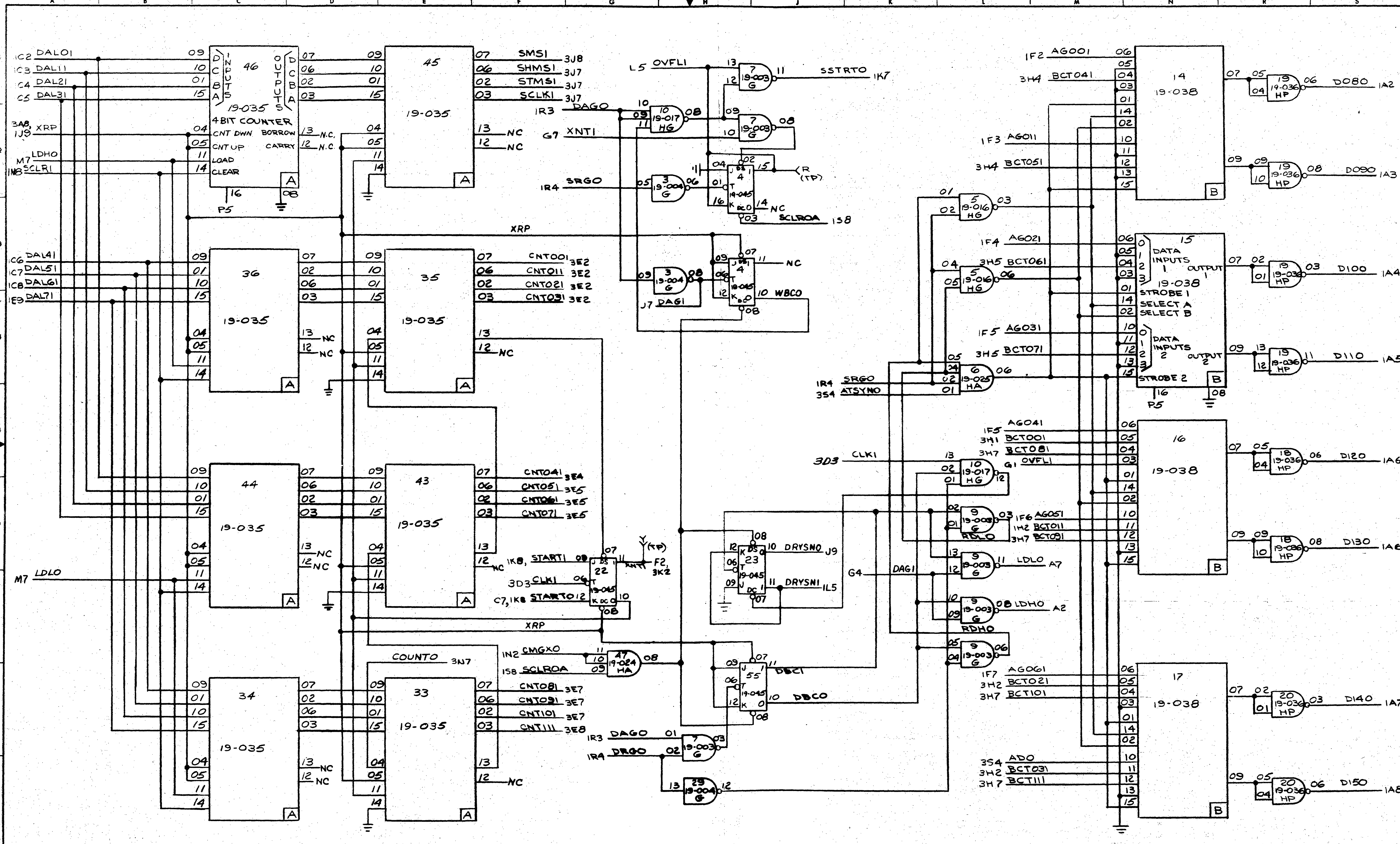
TITLE FUNCTIONAL SCHEMATIC UNIVERSAL CLOCK

03138

02-240R01D08

SHEET OF 1 - 4

INTERDATA®



NOTES

BRUNING 44 231 15043

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC UNIVERSAL CLOCK

03138

02-240R01 D08

SHEET 2-4

2J6 DRYSNO — 13 19-003 G

2J9 CLKO — 18 19-036 HP

11 19-035 4 BIT COUNTER — INPUTS D C B A; OUTPUTS D C B A; COUNT DWN; COUNT UP; LOAD; CLEAR; BORROW CARRY; P5; 08

CLK1 C6, C9, 1G8, 2J5

1K8 START1 — 22 19-045 — TMS1 J7

P5 R6 1K — 1K8 START0

21 19-035 — 07 NC; 06 NC; 02 NC; 03 NC; 13 NC; 12 NC

1K8 START1 — 1K8 START0 — D3 CLK1 — HMS1 J7

32 19-035 — 07 NC; 06 NC; 02 NC; 03 NC; 13 NC; 12 NC

1J8, 2A2, K2, L6 XRP

1K8 START1 — D3 CLK1 — 1K8 START0 — 23 19-045 — MSI J8

2G3 CNT001 — 2G3 CNT011 — 2G3 CNT021 — 2G4 CNT031 — LDBCO

25 19-035 — BCT001 2L5; BCT011 2L6; BCT021 2L8; BCT031 2L9; NC; NC

2G5 CNT041 — 2G6 CNT051 — 2G6 CNT061 — 2G6 CNT071

24 19-035 — BCT041 2L1; BCT051 2L2; BCT061 2L3; BCT071 2L4; NC; NC

2G8 CNT081 — 2G8 CNT091 — 2G8 CNT101 — 2G8 CNT111

26 19-035 — BCT081 2L5; BCT091 2L6; BCT101 2L8; BCT111 2L9; NC; NC

P5 R7 1K

1K1 ENAX1 — XATNI — 2 19-003 G

13 19-003 G — 20 19-036 HP — ATNO <223

A8 XRP — 2H6 XNTI — 19-045 HF — N.C.

1K2 XDSRM0 — S6 RXATNO — 2 19-003 G — C4 1000PF — 3 19-004 G

122 RACKO — R16 100 — R3 1K P5 — 60 19-004 G — 49 19-015 HG

1K5 ENAHI — HATNI — 2 19-003 G

S8 HNTI — 19-045 HF — NC

1K5 HDSRM0 — 2 19-003 G — 3 19-004 G — RHATNO

D 8 1 19-027 T L 0

60 19-004 G — 7 19-003 G — 13 19-003 G — 29 19-004 G

10 19-017 HG — TACKO <222

37 19-002 G

47 19-024 HA — 12 ATSYNO 2J5, 1K3, 1A8

27 19-003 G — AD0 2L8

P5 R13 6.8K — C2 47PF — 31 19-042 ONE SHOT — XRP — NC

P5 R14 6.8K — C3 47 PF — 31 19-042 ONE SHOT — NC — 04 RXATNO F3

53 19-026 — 2F1 SCLK1 — DG, 2F7 CLK1 — 2F1 STMSI — F4 TMSI — 2F1 SHMSI — F6 HMSI — 2F1 SMSI — F8 MSI — 08 S (TP) COUNTO 2E8

204-A C3 — 104-A C1 — D8 D9 D10 D11 — R8 470 — R9 470 — C1 .1MF — R10 1K — D12 — P5

R11 4.7K — Q1 — R12 180 — 3 19-004 G — 3 19-004 G — HNT1 J6

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

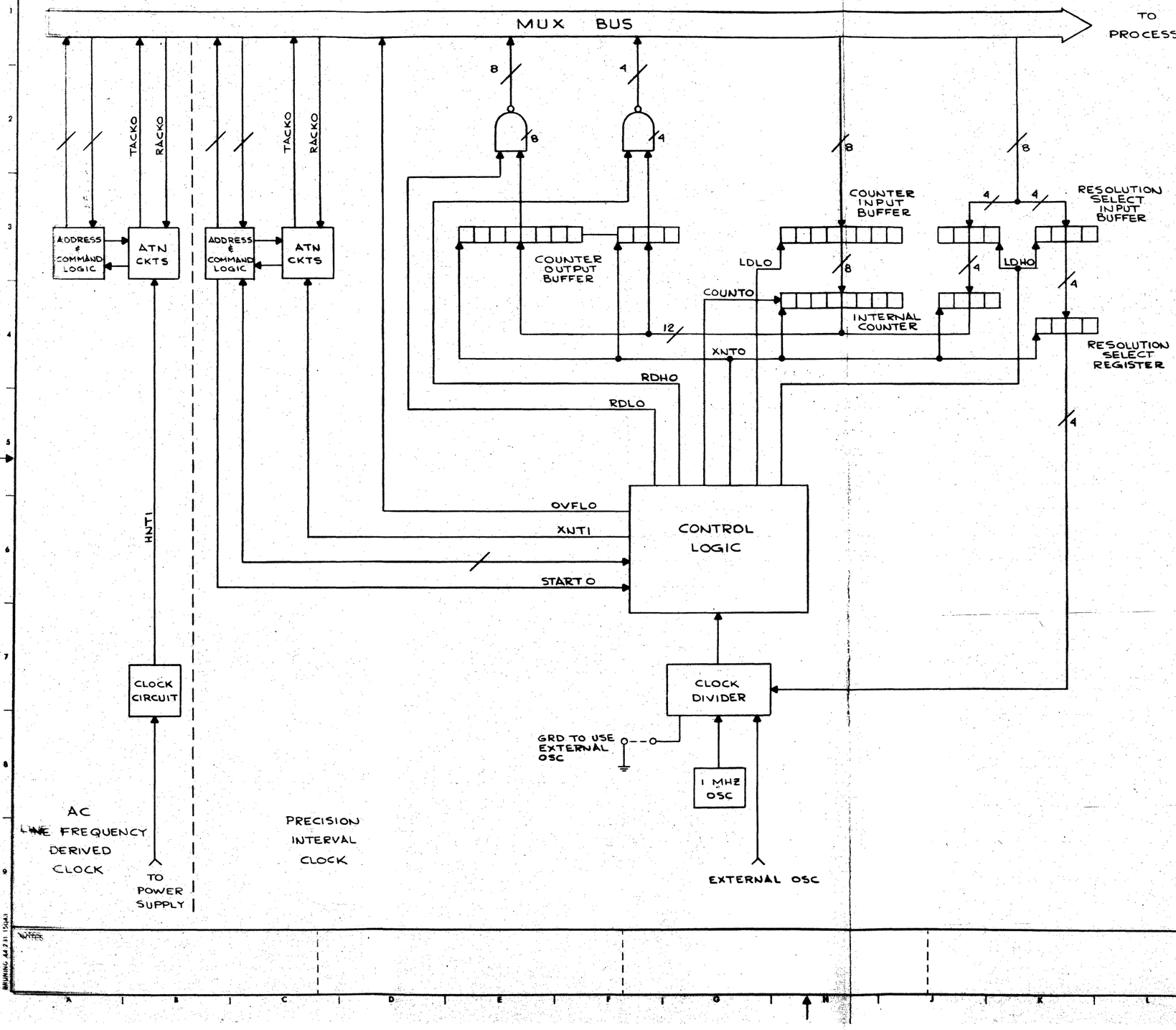
TITLE FUNCTIONAL SCHEMATIC UNIVERSAL CLOCK

SIZE 03138 — SHEET OF 3-4

DWG NO 02-240 R01 D08

BRUNING 44-231 15043

INTERDATA



BACK PANEL MAP

ROW 1	ROW 2	TERM NO.
P5	GND	41
		40
		39
		38
		37
		36
		35
		34
		33
		32
		31
		30
		29
		28
CLRO		27
STPCLRO		26
		25
		24
SYNO	ATNO	23
RACKO	TACKO	22
	DAO	21
DRO	CMDO	20
SRO	ADRSO	19
D14O	D15O	18
D12O	D13O	17
D10O	D11O	16
D08O	D09O	15
		14
		13
		12
		11
		10
		09
		08
		07
		06
		05
		04
		03
		02
		01
P5	GND	00

CONN 'A' PIN ASSIGNMENT

ROW 1	ROW 2	TERM NO.
C1	C3	04
		03
		02
		01
		00

TEST POINT INDEX

DESIG	MNEM	LOC
R	OVFLI	2H1
S	COUNTO	3M7
T	CLKO	1L9
Y	XNTI	2F2
Z	RCLKO	1H9
EXC		1G8
EXG		1G9

NOTES

NAME	TITLE	DATE	TITLE FUNCTIONAL SCHEMATIC
	DRAFT		UNIVERSAL CLOCK
	CHK		
	ENGR		
	DIR ENG		TASK NO. 03138
			DWG NO. 02-240 R01 D08
			SHEET 4 OF 4