PCP-177

GE-PAC* 30
CONTROL COMPUTER

MAINTENANCE MANUAL
30-2
VOLUME 2

GENERAL ELECTRIC

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GE-PAC 30
CONTROL COMPUTER

MAINTENANCE MANUAL
30-2
VOLUME 2

GENERAL ELECTRIC

1. INTRODUCTION

This Volume provides the drawings required to install, operate and maintain the Model 30-2. In addition, installation instructions are provided in this Volume.

2. INSTALLATION PROCEDURE

GENERAL ELECTRIC offers Installation service for the Model 30-2 System at its destination at published rates. To avail yourself of this service, contact your local GENERAL ELECTRIC representative when the system arrives. GENERAL ELECTRIC recommends that all systems be installed by our field service personnel. If GENERAL ELECTRIC installation service is not desired the following procedure should be followed.

CAUTION

To avoid damage to the Model 30-2 or its peripherals, read the following procedure before unpacking, installing, or applying power to the system.

1. Carefully remove each component from its carton or crate, observing any special unpacking instructions included with the component.

CAUTION

If a teletypewriter is included with the system, it must be gripped underneath the main part of its frame. The tape reader must not be used as a grip; it will not support the weight of the teletypewriter.

2. Inspect all components for physical damage.

3. If the system is to be rack mounted, secure the components in the rack. Refer to Sheet 1 of Drawing 70B113025 for mounting information.

4. If the system is received from GENERAL ELECTRIC already mounted in a cabinet or a rack, simply check to assure that the components are securely fastened.

5. If the system was shipped already mounted in a rack or cabinet, it is fully wired. Check that all terminals and connectors are secured properly, and skip steps 6 through 9.

6. If a Display Panel is included with the system, connect the cable to the appropriate positions on the Display Controller mother-board and location 40 on the Control 2 mother-board. (See Sheet 1 of Drawing 70B113025). Connect the power terminals to TB26 on the rear of the card file as shown on sheet 2 of Drawing 70B113025.

CAUTION

The wire color coding may vary on the TB26 terminals, i.e. a blue wire and a gray wire connected to the same terminal. To avoid damaging the equipment, rely on the terminals designations, not wire color when connecting the cables.

7. Connect the power supply cable to TB26 as shown on Sheet 2 of Drawing 70B113025.

8. Connect the power supply cable to TB4 and TB5 on the power supply as shown on sheet 3 of Drawing 70B113025.

9. Connect the AC power cable to TB1 on the power supply as shown on sheet 3 of Drawing 70A113025.

10. Use an ohmmeter to check for shorts between supply voltage terminals on the bus bar, and from the terminals to ground.

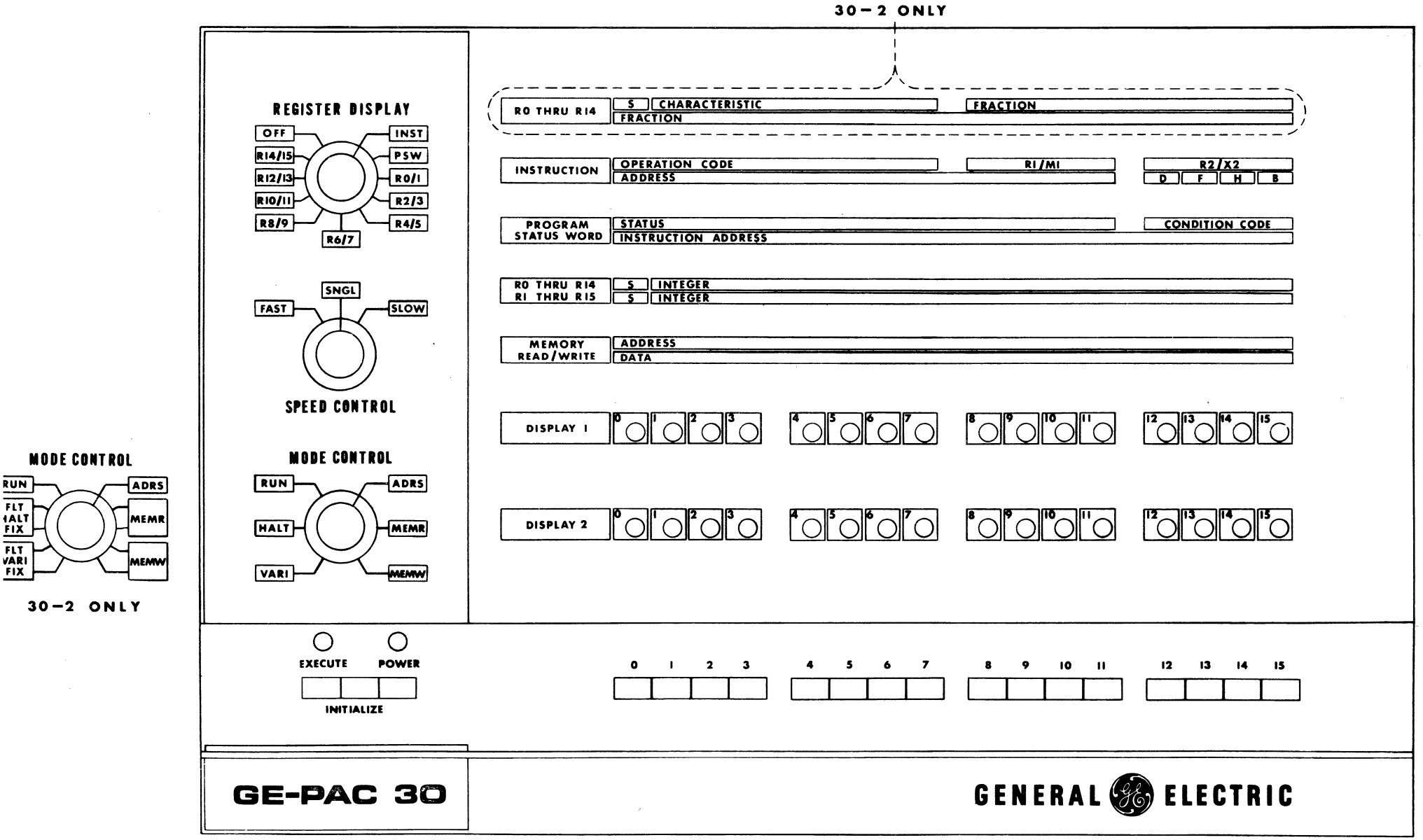
11. Assuming that the checks in Step 10 are satisfactory, apply power to the unit. The Model 30-2 Test Program supplied with each system may now be run to check the system's performance.

3. DRAWING INDEX

The following index lists the drawings provided in this basic manual. Note that additional drawings which further describe a particular system may be added at the end of the manual. The basic drawings are bound into the manual in the order listed in the following index.

DRAWING INDEX	DRAWING NUMBER
Display Panel Layout	NONE (REF. DWG)
30-2 Installation Specification	70B113025
Power Cable Wiring Diagram (Desk Top Cabinet)	70B113050
Power Cable Wiring Diagram (Systems Cabinet w/1 Expansion)	70B113052
Power Cable Wiring Diagram (Systems Cabinet w/2 or 3 Expansions)	70B113051
Mother-Board Information Drawing	70B113026
General Purpose Mother-Board Layout	NONE (REF. DWG)
Control and Display Cable Wiring	70C112550

Drawing Title	Drawing Number
emory Standard Interface	70B113000 (Sheets 0A, 1 Thru 7)
eletypewriter Interface functional Schematics	70B113002 (Sheets 0A,1 Thru 12)
isplay Controller functional Schematics	70B113003 (Sheets 0A,1 Thru 9)
ead Only Memory Switch	70B113004 (Sheets 0A,1 Thru 9)
OM Transformer	70B113005 (Sheets 0A,1 Thru 5)
ROM Transformer	70B113006 (Sheets 0A,1 Thru 7)
OM Interface	70B113007 (Sheets 0A,1 Thru 7)
rocessor Functional Schematics 30-2	70B113008 Sheets 0A,0B,1 Thru 31)
096 - 16 Bit Memory Block	70B113009 (Sheets 0A,1 Thru 27)
emory Parity and Protect	70B113010 Sheets 0A,1 Thru 8)
endor Power Supply Drawings	70B113065 (Sheets 1 Through 7)
rawing Number Conversion	None (Ref. Dwg.)



GE – PAC 30 OPERATORS CONSOLE

GENERAL ELECTRIC

PROCESS COMPUTERS
PHOENIX ARIZONA

TITLE

INSTALLATION SPECIFICATION

DRAWING NUMBER	CONT.	PAGE
70B113025	1	0

FIRST MADE FOR
GE-PAC 30
(3-109 R02 B12)

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
C	ISSUED				

REISSUED

C issued

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME

REISSUED

(3-109 R02 B12)

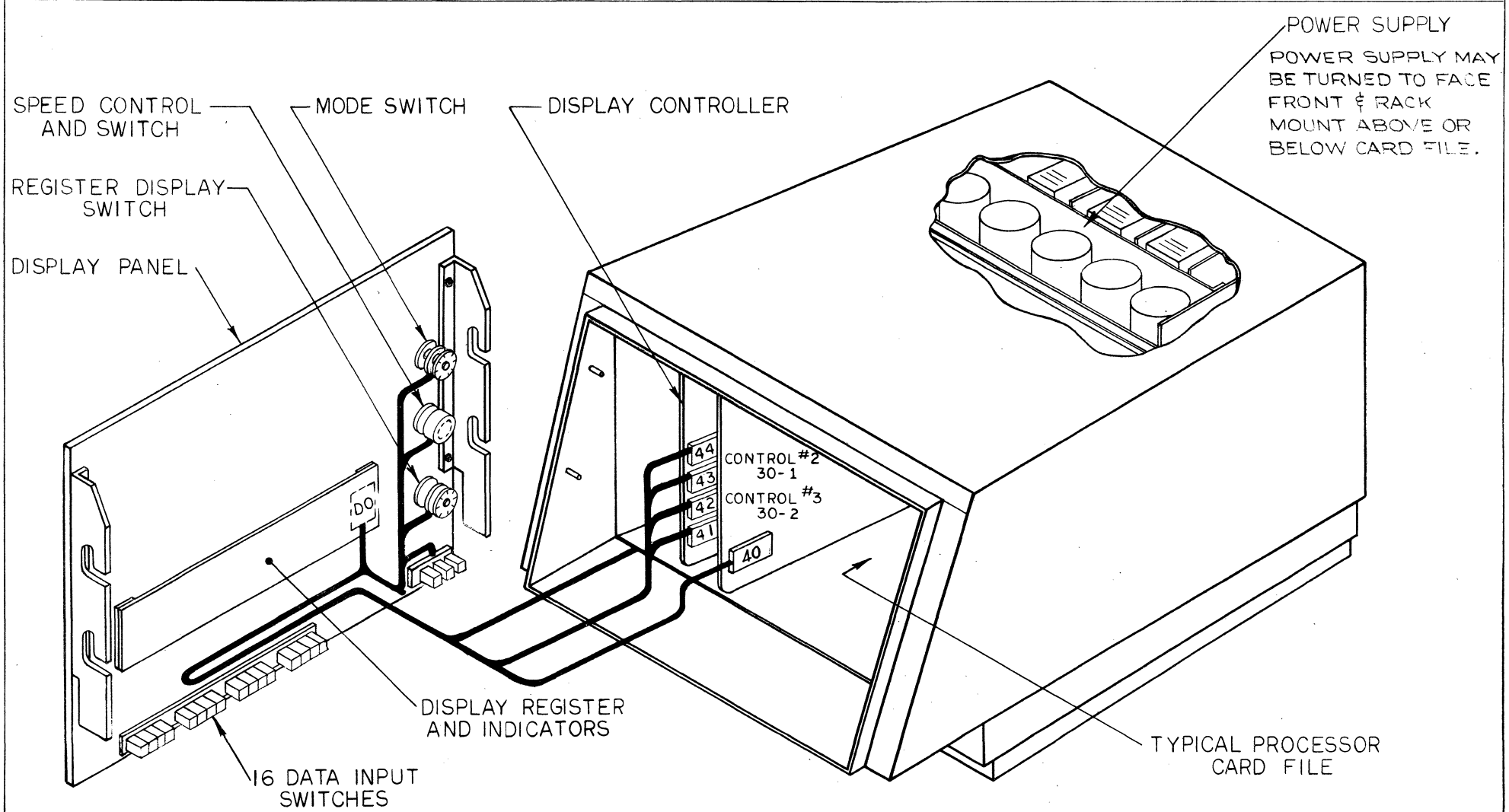
MADE BY	APPROVAL	REV.											
E. Ellsworth MAY 7, 69			C	Issued									
ISSUED													
July 18, 1969													

DWG. NO.	CONT.	PAGE
70B113025	1	0

PRINTS TO: K7-20

PCE 2981

DIST.	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—					GENERAL ELECTRIC	TITLE	DWG. NO.
K7-20	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS			PROCESS COMPUTER PHOENIX	INSTALLATION SPECIFICATION	(3-109 R02 B12)
			FRACTIONS	DECIMALS	ANGLES			70B113025
		√	±	±	±		FMF GE-PAC 30 1 FCF	CONT. ON SHEET 2 SH. NO. 1



MADE BY	APPROVAL												DWG. NO.
E. Ellsworth MAY 7, '69	E. G. White July 17, 69	DES.		REV.									(3-109 R02 B12)
ISSUED		CHKR.	DR										70B113025
July 18, 1969													CONT ON SHEET 2 SH NO. 1

DIST.	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—					GENERAL ELECTRIC	TITLE	DWG. NO. (3-109 R02 B12)
K7-20	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES	PROCESS COMPUTER PHOENIX	INSTALLATION SPECIFICATION	70B113025
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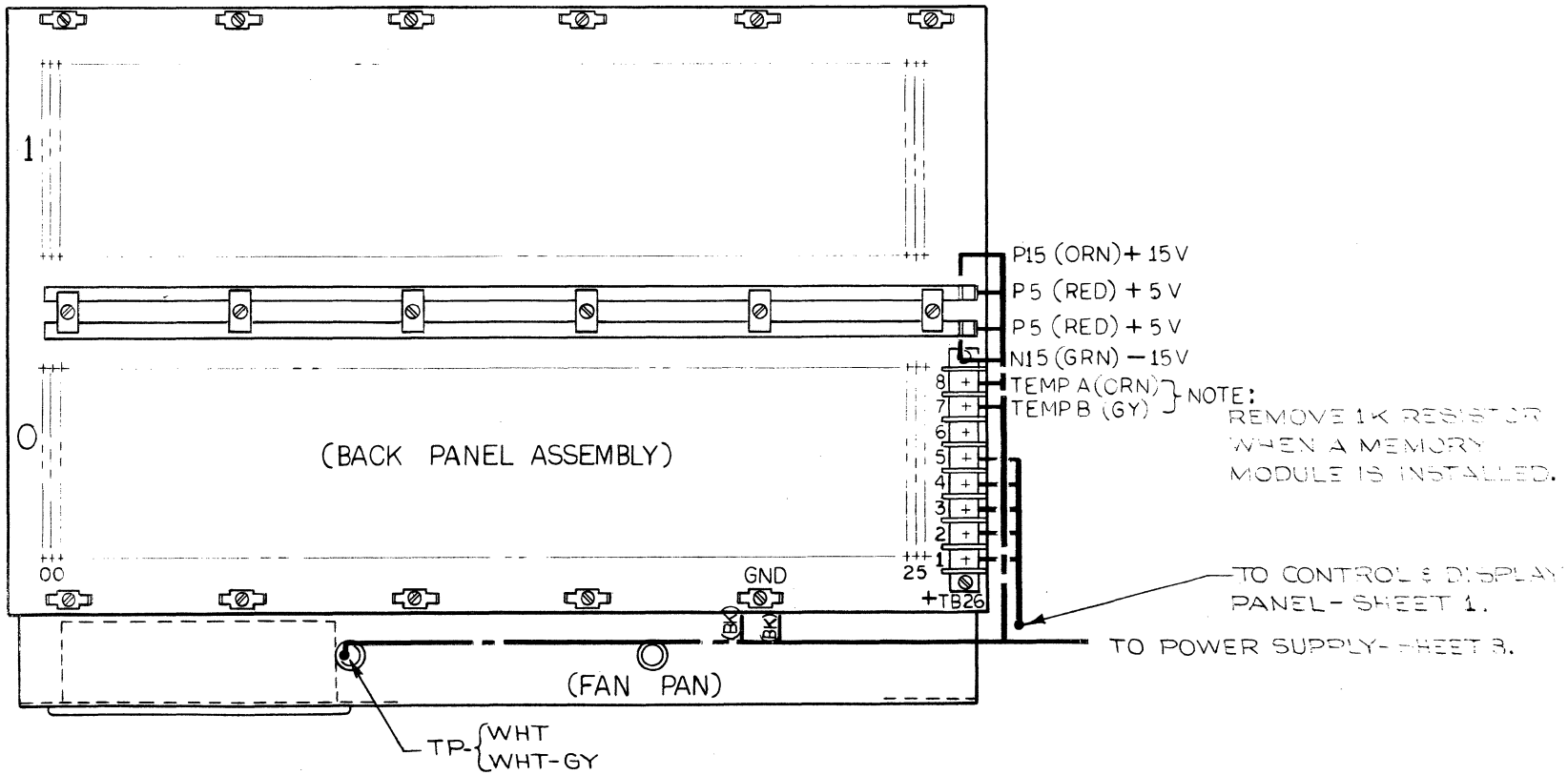
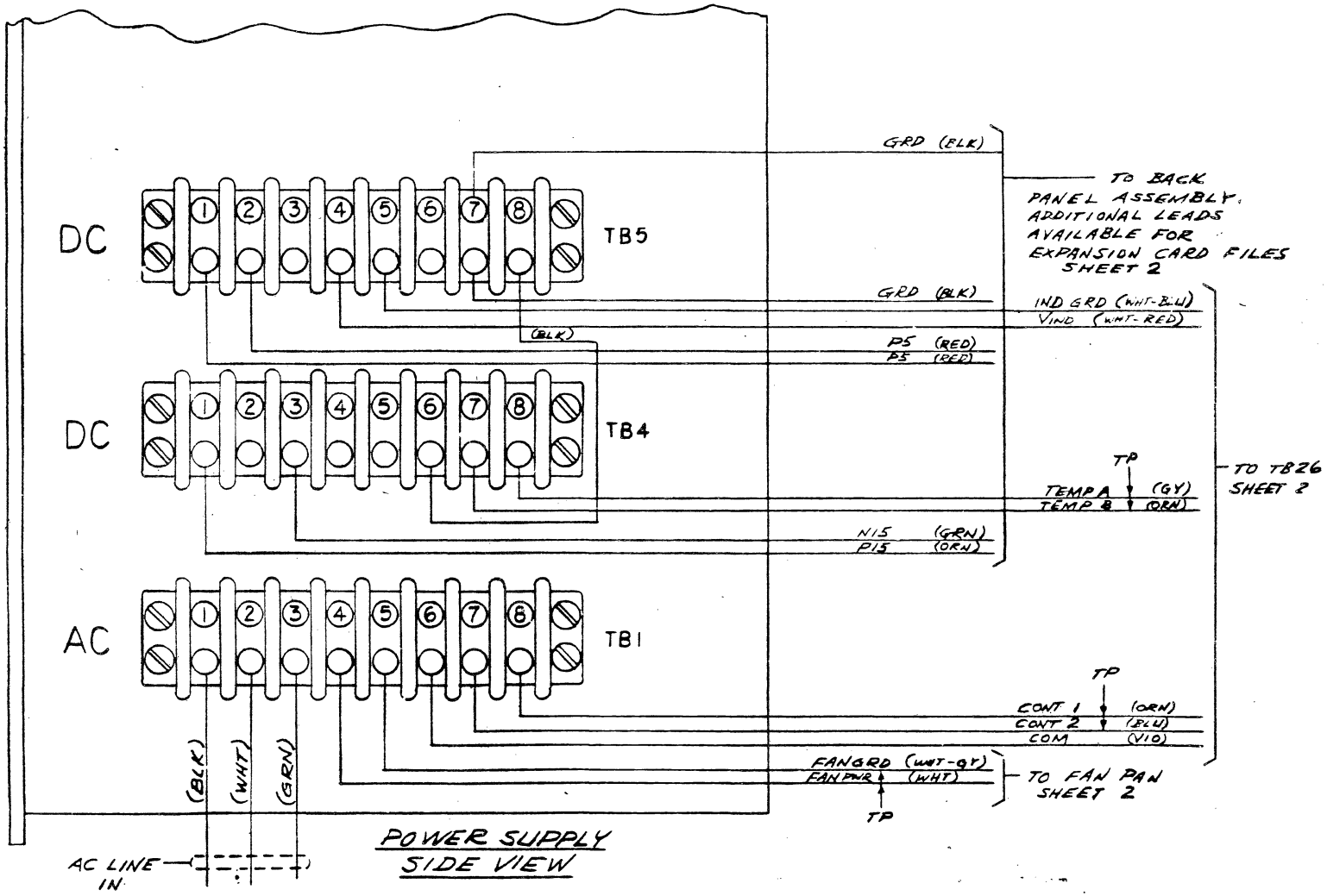


REAR VIEW

CABLE PATH SHOWN
FOR PROCESSOR
CARD FILE

MADE BY	APPROVAL											DWG. NO. (3-109 R02 B12)
C. Gilmith. JUN. 26, '69	DK E. G. White July 17, 69	DES.		REV.								70B113025
ISSUED July 18, 1969		CHKR.	DK									CONT ON SHEET 3 SH NO. 2

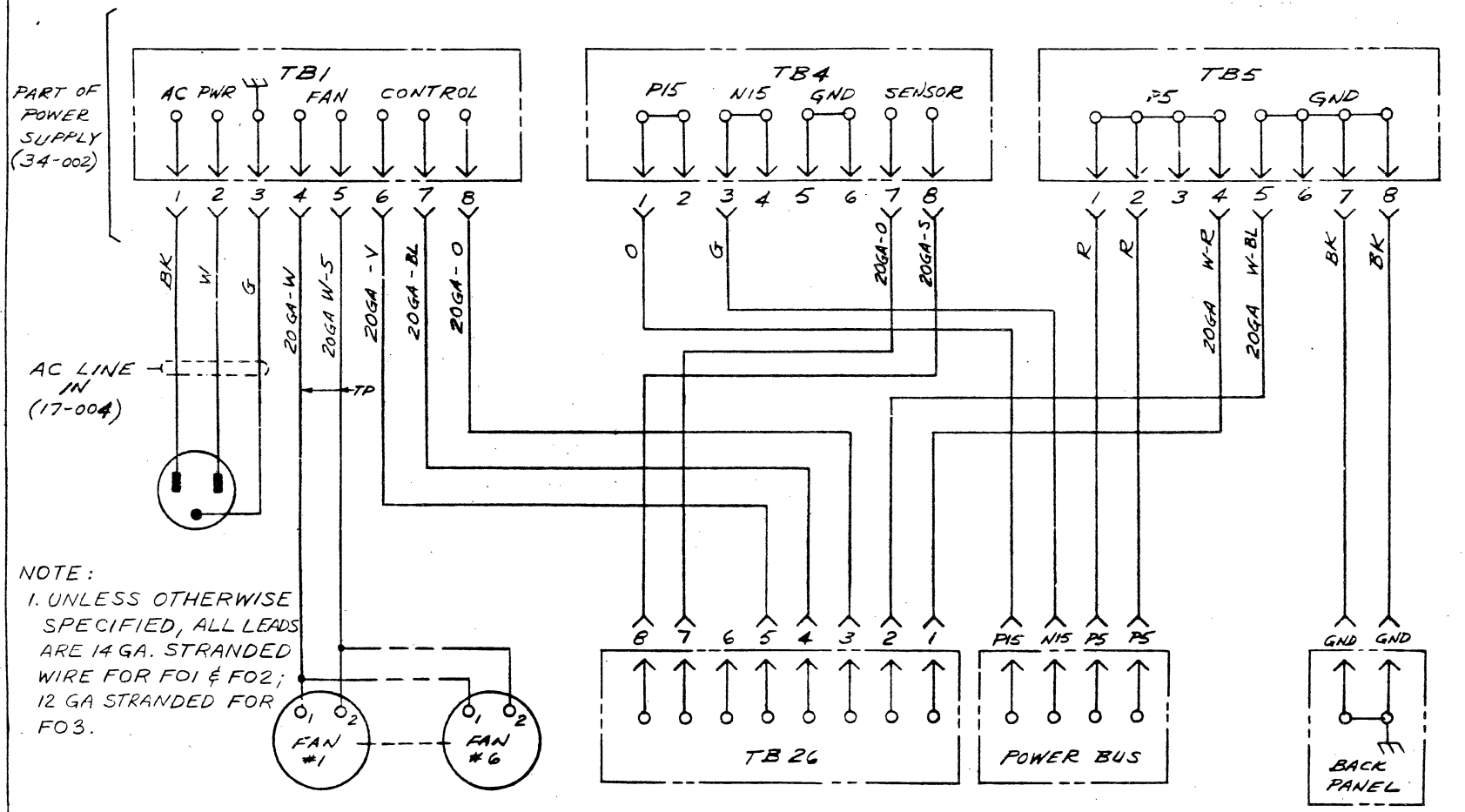
DIST.	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—					GENERAL ELECTRIC	TITLE	DWG. NO. (3-109 R02 B/2)
K7-12	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES	PROCESS COMPUTER PHOENIX	MODEL 3 INSTALLATION SPECIFICATION	70B113025
		√	±	±	±		FMF GE-PAC 30 | FCF	CONT. ON SHEET F SH. NO. 3



POWER SUPPLY SIDE VIEW

MADE BY	APPROVAL			REV.			DWG. NO. (3-109 R02 B/2)
J.M.C. Avery JUNE 27, 69	DR E.G. White July 17, 69	DES.		C	ISSUED		70B113025
ISSUED July 18, 1969		CHKR.	DR				CONT ON SHEET F SH NO. 3

DIST.	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—					GENERAL ELECTRIC	TITLE	DWG. NO.
K7-06	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES	PROCESS COMPUTER PHOENIX	CABLE WIRING DIAGRAM, PROCESSOR POWER	(17-011 R01 B06) 70B113050
		√	±	±	±		FMF GE-PAC 30 1 FCF	CONT. ON SHEET F SH. NO. 1



NOTE:
1. UNLESS OTHERWISE SPECIFIED, ALL LEADS ARE 14 GA. STRANDED WIRE FOR FO1 & FO2; 12 GA STRANDED FOR FO3.

MADE BY	APPROVAL			REV.			DWG. NO.
J. Kitzajian JUNE 27, 69	P. G. White July 17, 69	DES.		B	ISSUED		(17-011 R01 B06) 70B113050
ISSUED July 18, 1969		CHKR.	DR				CONT ON SHEET F SH NO. 1

DIST KT-06

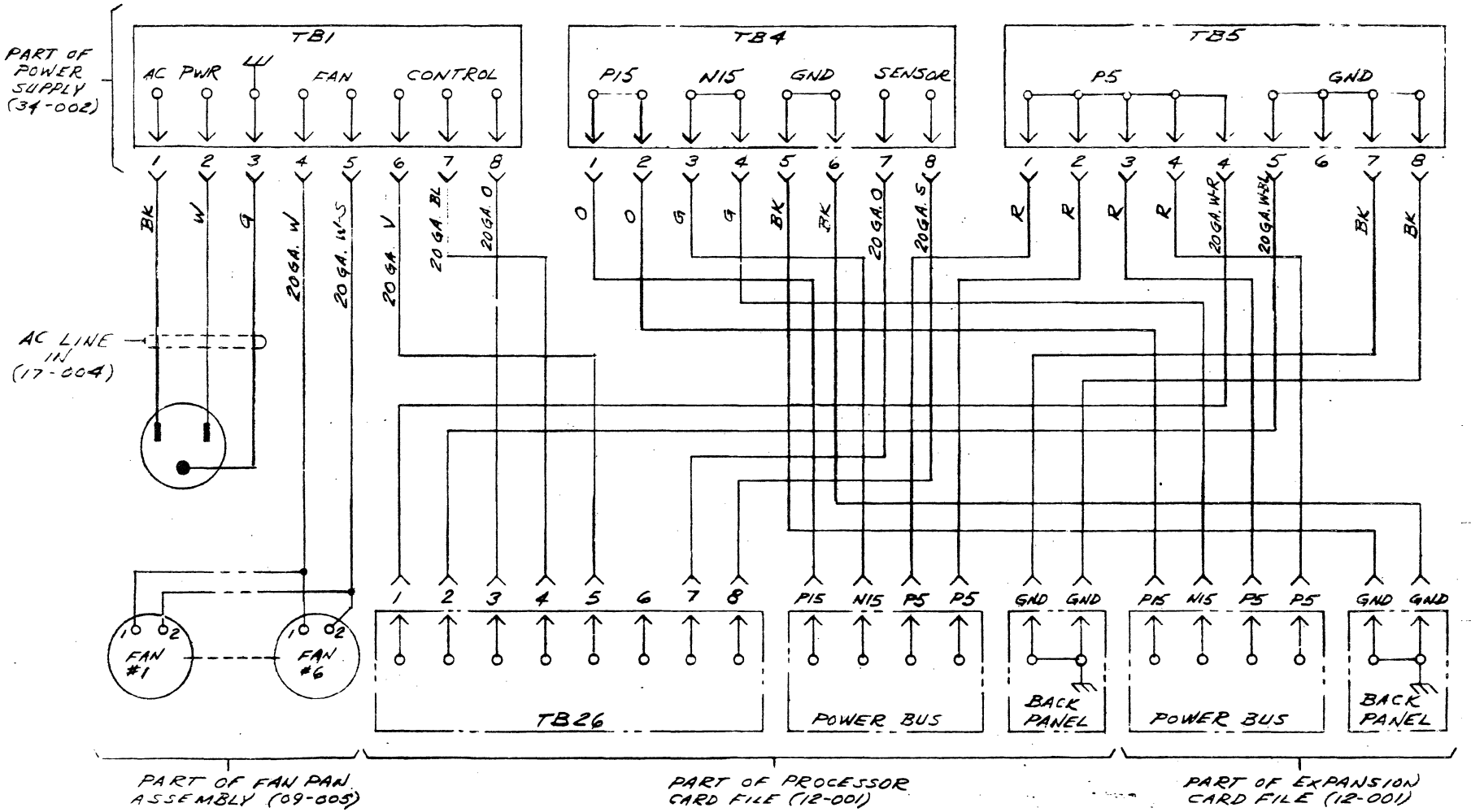
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES: V | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE CABLE WIRING DIAGRAM
POWER-SYSTEM CABINET
FMF GE-PAC 30 | FCF

DWG. NO. (17-039 B06) 70B113052
CONT. ON SHEET F SH. NO. 1

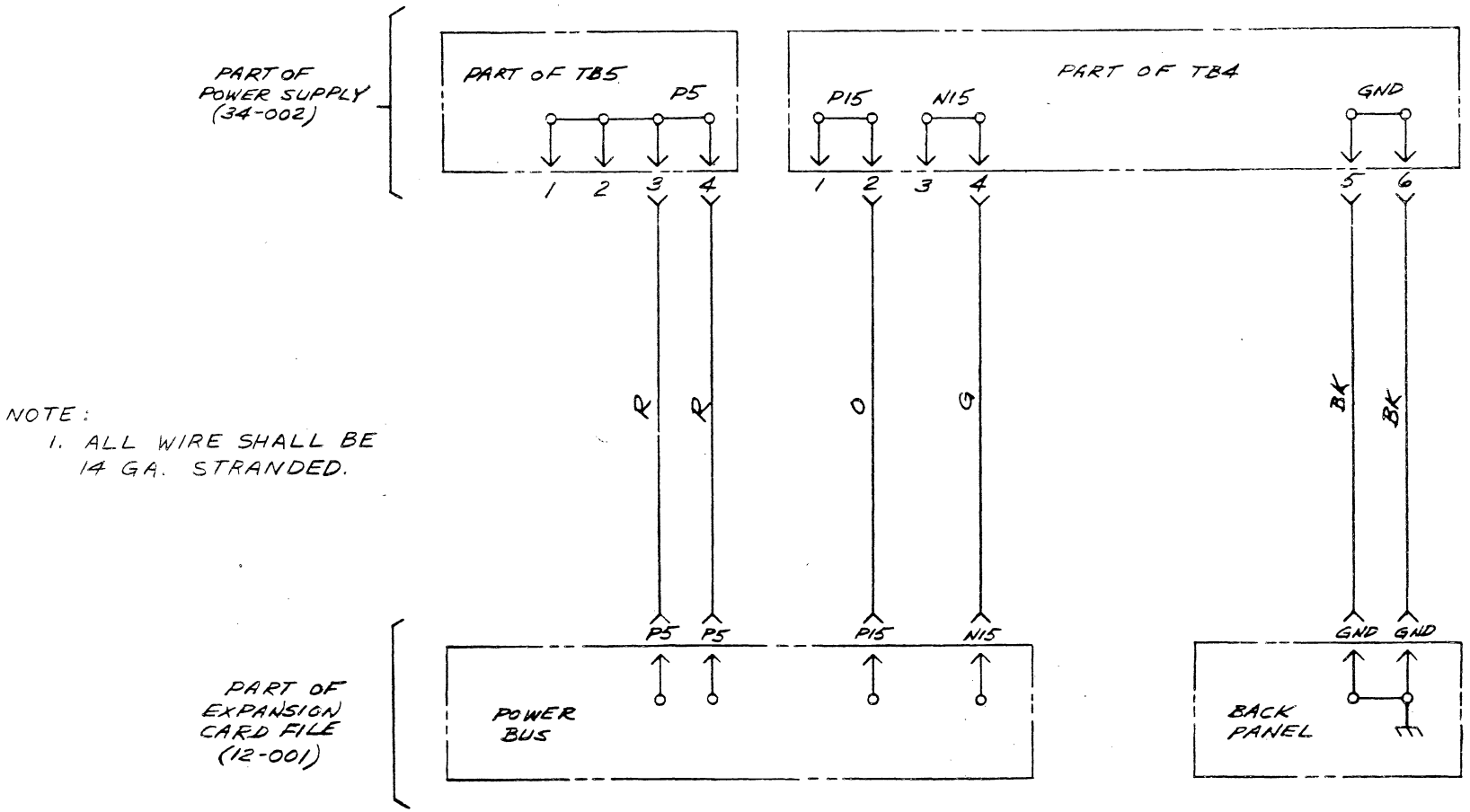
NOTES: 1- UNLESS OTHERWISE SPECIFIED, ALL LEADS SHALL BE 14GA. STRANDED WIRE.



MADE BY J. McAvoy JUNE 27, '69
ISSUED July 18, 1969
APPROVAL DR E. G. White July 17, 69
DES. | CHKR. DR
REV. A ISSUED

DWG. NO. (17-039 B06) 70B113052
CONT ON SHEET F SH. NO. 1

DIST.	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING: —					GENERAL ELECTRIC	TITLE	DWG. NO. (17-024 R01 B06)
K7-06	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES	PROCESS COMPUTER PHOENIX	CABLE WIRING DIAGRAM EXPANSION POWER	70B113051
		√	±	±	±		FMF GE-PAC 30 1 FCF	CONT. ON SHEET F SH. NO. 1



NOTE:
1. ALL WIRE SHALL BE 14 GA. STRANDED.

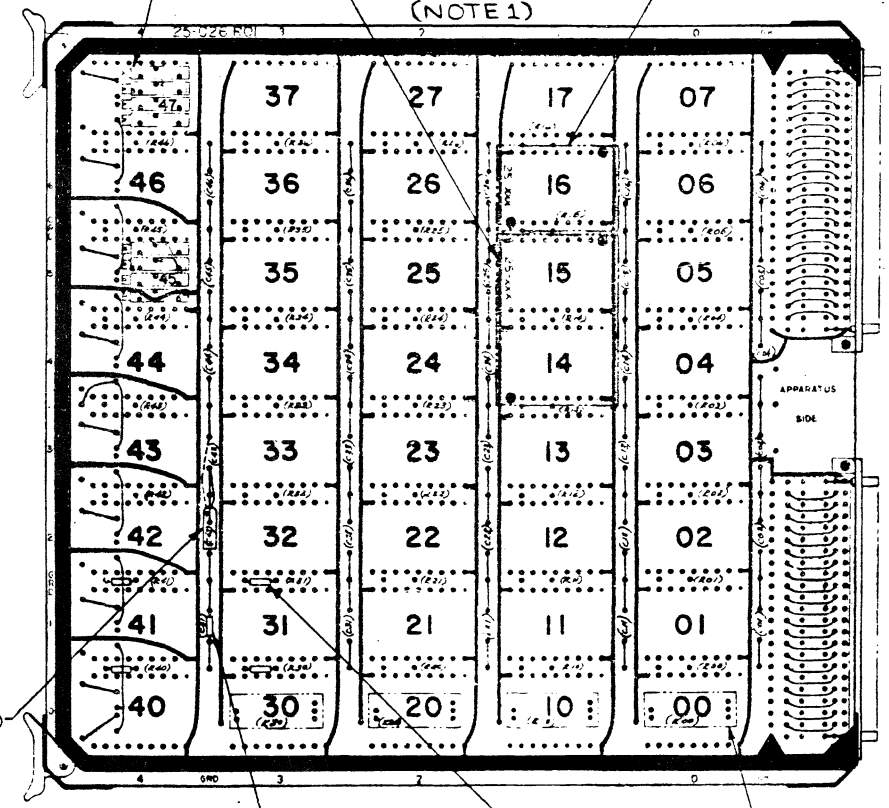
MADE BY	APPROVAL			REV.			DWG. NO (17-024 R01 B06)
J. Kitajima JUNE 27, 69		DES.		MB	ISSUED		70B113051
ISSUED July 18, 1969		CHKR.	GR				CONT ON SHEET F SH NO. 1

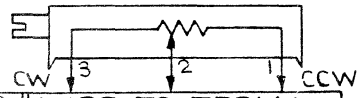
DIST.	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—					GENERAL ELECTRIC	TITLE	DWG. NO (35-050 C12)
K7-20	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ±	DECIMALS ±	ANGLES ±	PROCESS COMPUTER PHOENIX	INFORMATION GENERAL PURPOSE ASM (FMF / FCF)	70B113026 CONT. ON SHEET F SH. NO. 1
		√						

21-003 FOI TRIMPOT (PXX1)(PXX2)(PXX3)(PXX4) 8 POSITIONS AVAILABLE; LOCATE AS SHOWN. (NOTES 1 & 3)

#3 DAUGHTER BOARD ASM-TYP LOCATION (XX) SPECIFIED BY THE LOWER OF TWO POSITIONS OCCUPIED (NOTE 1)

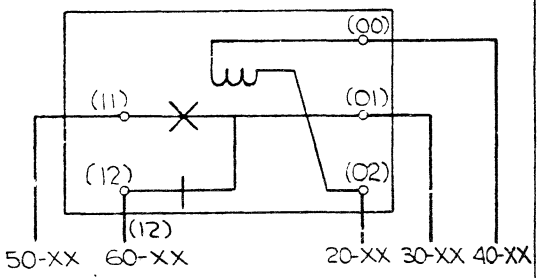
#2 DAUGHTER BOARD ASM. (XX)- TYP (NOTE 1)





FOR:	WIRE TO TERM:		
P474	51-47	31-47	11-47
P473	61-47	41-47	21-47
P472	60-47	40-47	20-47
P471	50-47	30-47	10-47
P454	51-45	31-45	11-45
P453	61-45	41-45	21-45
P452	60-45	40-45	20-45
P451	50-45	30-45	10-45

TYP WIRING:



NOTES:
1. ALL ADDITIONAL APPARATUS SHALL BE SPECIFIED BY LOCATION ON 32-XXX ASM PARTS LISTS.
2. UNLESS OTHERWISE SPECIFIED, ALL CAPACITOR POS.(+) AND ALL DIODE CATHODES(‡) SHALL POINT TOWARDS THE TOP OF THE BOARD.
3. MOUNTING OF ANY TRIMPOT OR RELAY ELIMINATES USE OF THAT POSITION AS A DAUGHTER BOARD LOCATION.

MF VALUED CAPACITORS MAY BE MOUNTED ACROSS EITHER ONE OR TWO (XXR) POSITIONS AS SHOWN; OPTIONAL DOTTED LEAD MUST HAVE INSULATED SLEEVE (NOTES 1 & 2)

30 (CXX) POSITIONS- TYP FOR:
RESISTORS- ¼ W
CAPACITORS - PF VALUE
DIODES - WG 142
(NOTES 1 & 2)

1K, ¼ W RESISTORS (35 AVAIL) TYP REF: MOUNTED AS PART OF ASM 35-050 C03; REMOVAL SHALL BE SPECIFIED ON 32-XXX ASM PARTS LIST PER LOCATION (RXX).

36-001 REED RELAY SPDT 4 (KXX) POSITIONS AVAILABLE. (NOTES 1 & 3)

MADE BY	APPROVAL									DWG. NO. (35-050 C12)
C. Ellsworth JUN. 27, '69	E. G. White Jul. 17, 69	DES.		MA	ISSUED					70B113026
ISSUED July 18, 1969		CHKR.								CONT ON SHEET F SH NO. 1

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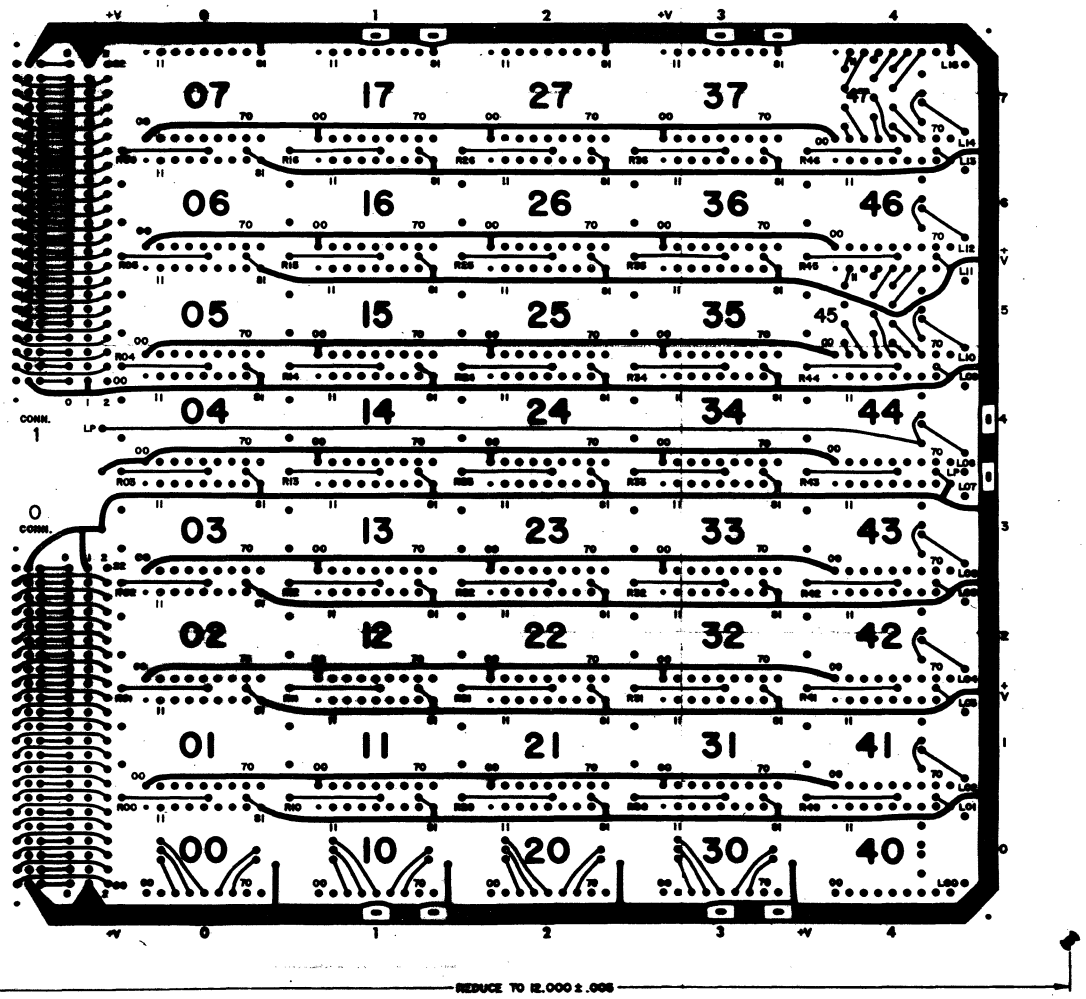
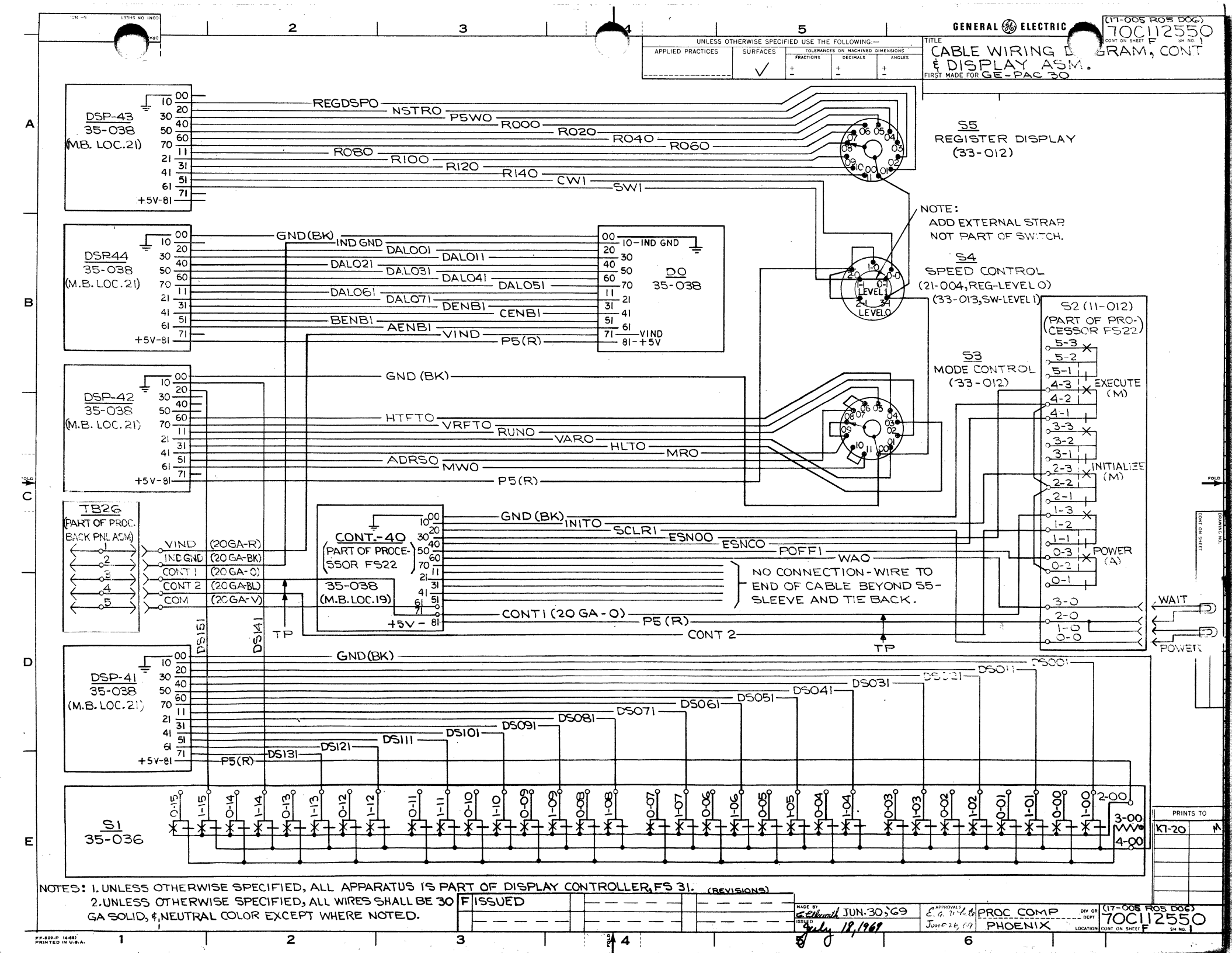
FIRST MADE FOR GE-PAC 30



REVISIONS	PRINTS TO

DRAWN BY Dennis Eythorne JUN 27,1969 ISSUED	APPROVALS	PROCESS COMPUTER DEPT PHOENIX, ARIZ.	REF DWG


GENERAL ELECTRIC
(17-005 ROS DOC) 70C112550 CONT ON SHEET F SH NO 1
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES
SURFACES
TOLERANCES ON MACHINED DIMENSIONS
FRACTIONS
DECIMALS
ANGLES
TITLE
CABLE WIRING DIAGRAM, CONT
& DISPLAY ASM.
FIRST MADE FOR GE-PAC 30
DSP-43
35-038
(M.B. LOC.21)
REGDSPO
NSTRO
P5WO
R000
R020
R040
R060
R080
R100
R120
R140
CW1
SW1
+5V-81
S5
REGISTER DISPLAY
(33-012)
NOTE:
ADD EXTERNAL STRAP
NOT PART OF SWITCH.
DSP44
35-038
(M.B. LOC.21)
GND(BK)
IND GND
DALO01
DALO11
DALO21
DALO31
DALO41
DALO51
DALO61
DALO71
DENB1
CENB1
BENB1
AENB1
VIND
P5(R)
DO
35-038
VIND
81-+5V
S4
SPEED CONTROL
(21-004, REG-LEVEL 0)
(33-013, SW-LEVEL 1)
LEVEL 1
LEVEL 0
S2 (11-012)
(PART OF PROCESSOR FS22)
S3
MODE CONTROL
(33-012)
EXECUTE (M)
INITIALIZE (M)
POWER (A)
WAIT
POWER
DSP-42
35-038
(M.B. LOC.21)
GND (BK)
HTFTO
VRFTO
RUNO
VARO
HLTO
MRO
ADRSO
MWO
P5(R)
TB26
(PART OF PROC. BACK PNL ASM)
VIND (20GA-R)
IND GND (20 GA-BK)
CONT 1 (20 GA-O)
CONT 2 (20GA-BL)
COM (20GA-V)
CONT.-40
(PART OF PROCESSOR FS22)
35-038
(M.B. LOC.19)
GND (BK)
INIT0
SCLR1
ESN00
ESNC0
POFF1
WA0
NO CONNECTION - WIRE TO END OF CABLE BEYOND S5 - SLEEVE AND TIE BACK.
CONT 1 (20 GA - O)
P5 (R)
CONT 2
TP
TP
DSP-41
35-038
(M.B. LOC.21)
GND(BK)
DS151
DS141
DS131
DS121
DS111
DS101
DS091
DS081
DS071
DS061
DS051
DS041
DS031
DS021
DS011
DS001
P5(R)
S1
35-036
3-00
4-00
PRINTS TO
K1-20
NOTES: 1. UNLESS OTHERWISE SPECIFIED, ALL APPARATUS IS PART OF DISPLAY CONTROLLER, FS 31.
2. UNLESS OTHERWISE SPECIFIED, ALL WIRES SHALL BE 30 GA SOLID, &, NEUTRAL COLOR EXCEPT WHERE NOTED.
(REVISIONS)
F ISSUED
MADE BY
ISSUED JUN.30,'69
APPROVALS
July 18, 1969
PROC COMP
PHOENIX
(17-005 ROS DOC) 70C112550 CONT ON SHEET F SH NO 1
FF-809-P (4-68) PRINTED IN U.S.A.

GENERAL ELECTRIC

PROCESS COMPUTERS
PHOENIX ARIZONA

TITLE

FUNCTIONAL SCHEMATIC, MEMORY STANDARD INTERFACE

DRAWING NUMBER	CONT.	PAGE
70B113000	0A	0

FIRST MADE FOR
GE-PAC 30 PROJECT

(FS28)

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
E	ISSUED				

REISSUED

E Issued

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME

REISSUED

(FS 28)

MADE BY	APPROVAL	REV.		DWG. NO.	CONT.	PAGE
C. Ellsworth JUN 17,'69	E. G. Zukle June 24, 69	E		70B113000	0A	0
ISSUED				PRINTS TO: K7-08		
July 18, 1969						

PCE 2981

DIST.	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING					GENERAL ELECTRIC	TITLE FUNCTIONAL SCHEMATIC	DWG NO (FS 28)
	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES	PROCESS COMPUTER PHOENIX	MEMORY STANDARD INTERFACE	70B113000
		√	±	±	±		FMF GE-PAC 30 PROJECT 1 FCF	CONT ON SHEET 1 SH NO 0A

SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
SHEET INDEX SUPPORTING INFORMATION	0A	-	-	3	4																
MEMORY ADDRESS REGISTER HIGH	1	-	-	3	3																
MEMORY ADDRESS REGISTER LOW	2	-	-	3	3																
MEMORY DATA REGISTER HIGH	3	-	-	3	3																
MEMORY DATA REGISTER LOW	4	-	-	3	3																
TIMING	5	-	-	3	4																
LOAD CONTROL	6	-	-	3	3																
BACK PANEL MAP	7	-	-	3	3																
ISSUE DATE				8-7-68	1-15-69																

SUPPORTING INFORMATION

CATEGORY	PART NO.
MOTHER BOARD MEMORY STANDARD INTERFACE	32-044R02

SHEET INDEX NOTES:

1. CHANGES ON THIS DRAWING SHALL REQUIRE ONLY THE REISSUE OF SHEETS AFFECTED.
2. THE ISSUE OF THIS SHEET SHALL DETERMINE THE LATEST ISSUE OF THIS DRAWING.

(FS28)

MADE BY	APPROVAL				DWG. NO.
E. Ellsworth JUNE 17, '69	E. G. White June 26, 69	DES.	REV.	E	70B113000
ISSUED JUL 18 1969		CHKR. OR			CONT ON SHEET 1 SH NO 0A

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING: –

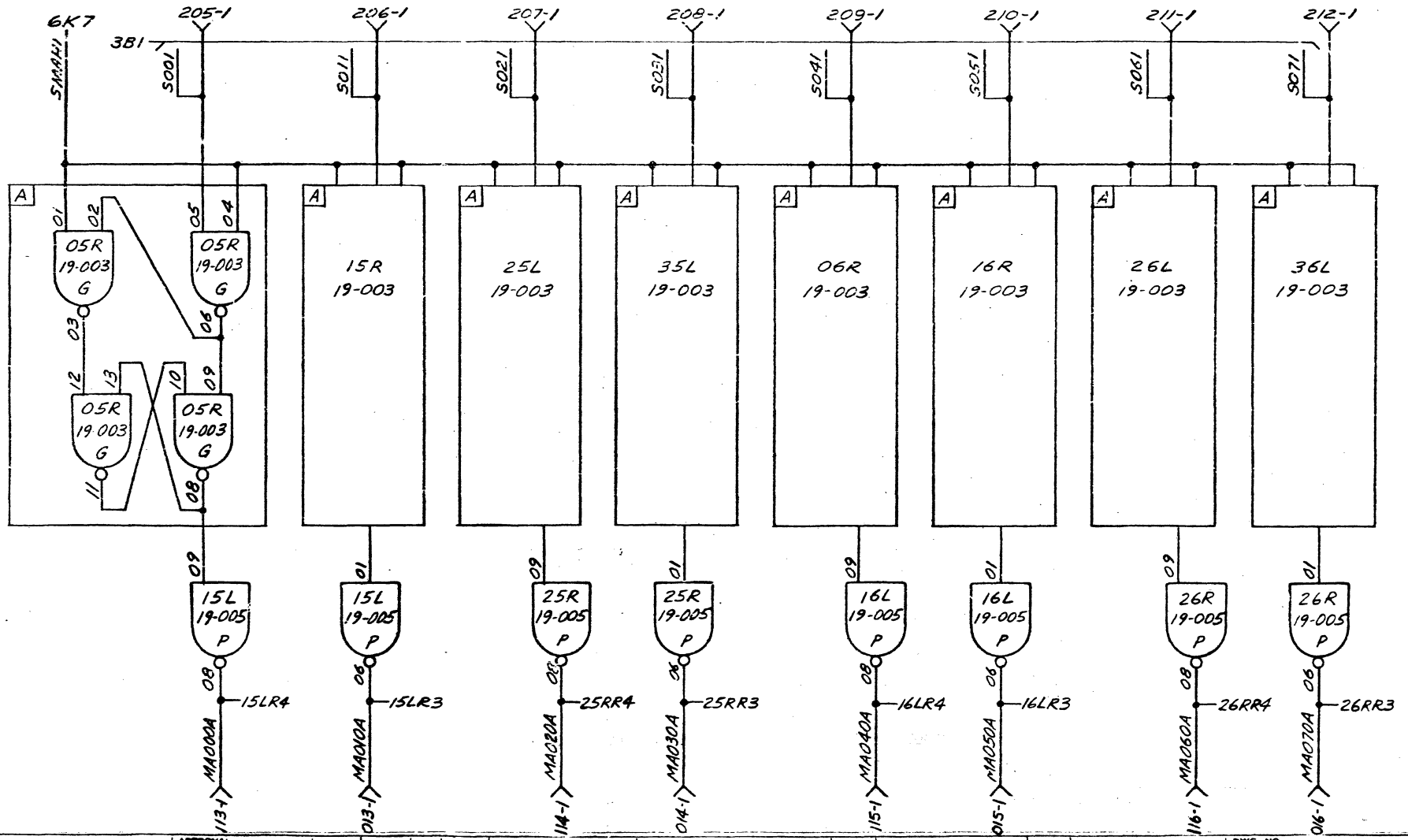
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	V	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
MEMORY STANDARD INTERFACE
FMF GE-PAC 30 | FCF

DWG. NO. (FS 28) 70B113000
CONT. ON SHEET 2 SH. NO 1

MEMORY AUDRESS REGISTER HIGH



MADE BY	APPROVAL				
G. Ellsworth JUNE 17, 1969	E.A. White June 26, 69	DES.		REV.	E
ISSUED JUL 18 1969		CHKR.	DR		

DWG. NO. 70B113000 (FS28)
CONT ON SHEET 2 SH NO. 1

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

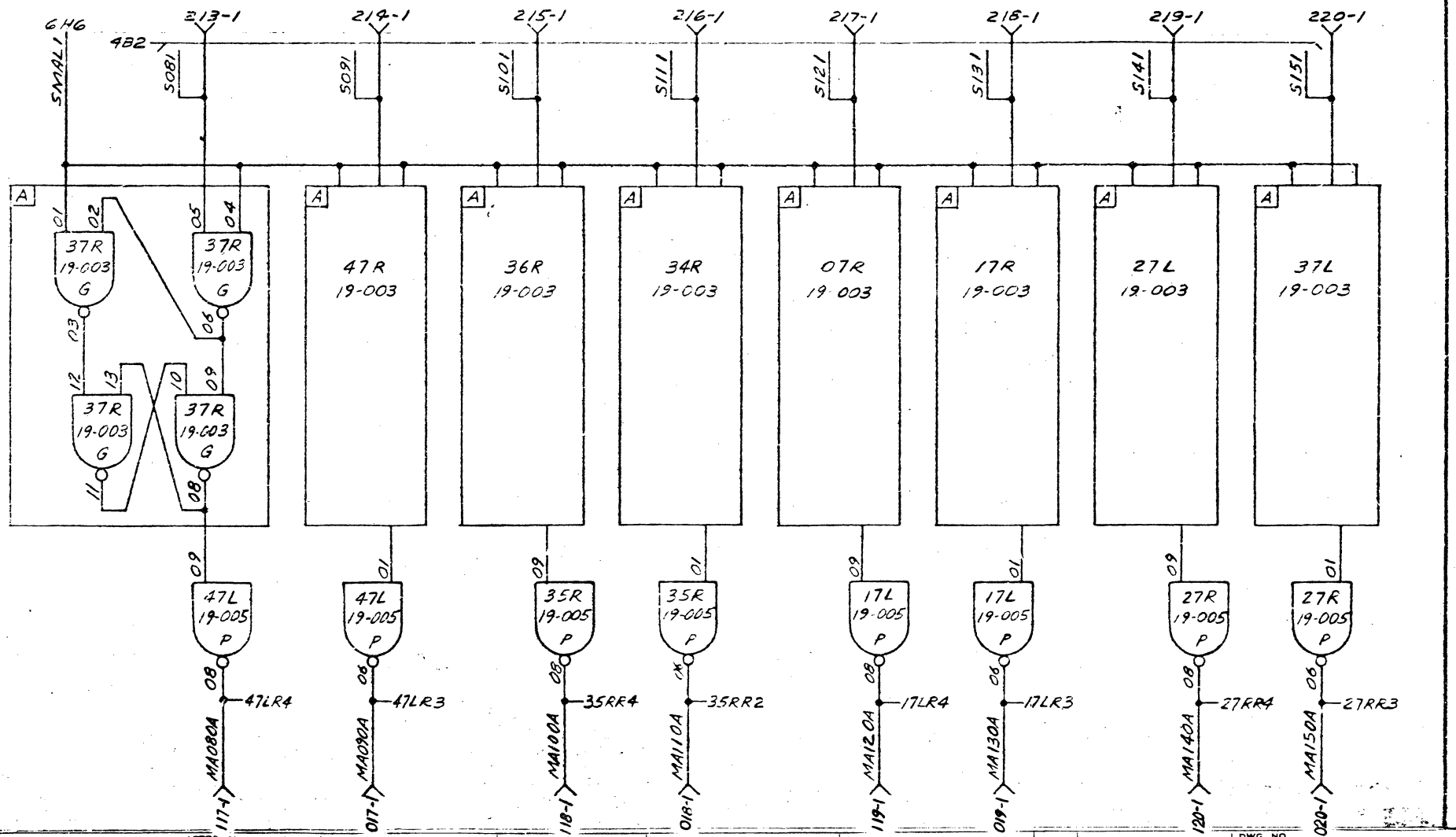
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
MEMORY STANDARD INTERFACE
FM-GE-PAC 30 | FCF

DWG NO (FS28) 70B113000
CONT. ON SHEET 3 SH NO 2

MEMORY ADDRESS REGISTER LOW



MADE BY E. Ellsworth JUN 17, 1969
ISSUED JUL 18 1969

APPRO. AL E. G. White June 26, 69
DES.
CHKR. DR
REV E

DWG NO (FS28) 70B113000
CONT ON SHEET 3 SH NO. 2

DIST.

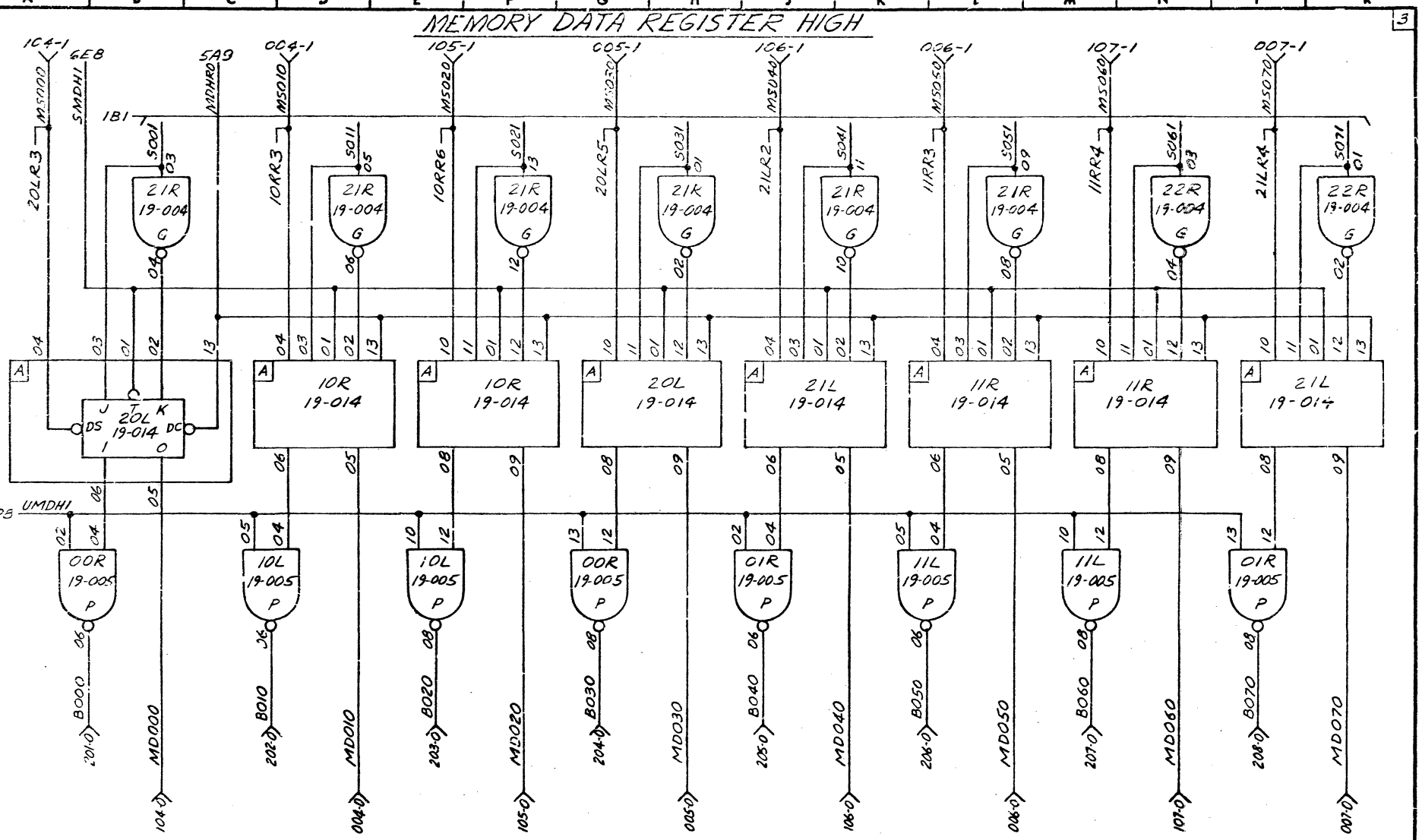
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
MEMORY STANDARD INTERFACE
FMF GE-PAC 30 | FCF

DWG. NO. (FS28) 70B113000
CONT. ON SHEET 4 SH. NO 3

MEMORY DATA REGISTER HIGH



MADE BY C. Ellsworth JUNE 17, 1969
ISSUED JUL 18 1969

APPROVAL E. G. White June 26, 69

DES. | CHKR. DR | REV. E

DWG. NO (FS28) 70B113000
CONT ON SHEET 4 SH NO. 3

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
MEMORY STANDARD INTERFACE
FMF GE-PAC 30 | FCF

DWG NO (FS28) 70B113000
CONT ON SHEET 5 SH NO 4

MEMORY DATA REGISTER LOW

3

108-1 6B8 SMALL 1
113-0 MDLR0 5F7
008-1 009-1 010-1 011-1

MS080 MS090 MS100 MS110 MS120 MS130 MS140 MS150

2B1

22LR3 12RR3 12RR5 22LR6 23LR3 13RR3 13RR4 23LR4

S091 S101 S111 S121 S131 S141 S151

22R 19-004 G
23R 19-004 G

22L 19-014 (J T K, DS, DC, I, O)
12R 19-014
22L 19-014
23L 19-014
13R 19-014
13R 19-014
23L 19-014

6N8 UMDL1

02R 19-005 P
12L 19-005 P
02R 19-005 P
03R 19-005 P
13L 19-005 P
13L 19-005 P
03R 19-005 P

B080 B090 B100 B110 B120 B130 B140 B150

209-0 210-0 211-0 212-0 213-0 214-0 215-0 216-0

MD080 MD090 MD100 MD110 MD120 MD130 MD140 MD150

108-0 008-0 109-0 009-0 110-0 010-0 111-0 011-0

MADE BY	APPROVAL			
C. Ellsworth JUN 17, 1969	E. G. White June 26, 69	DES.	REV.	E
ISSUED JUL 18 1969		CHKR. DR		

DWG. NO. (FS28) 70B113000
CONT ON SHEET 5 SH NO 4

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—

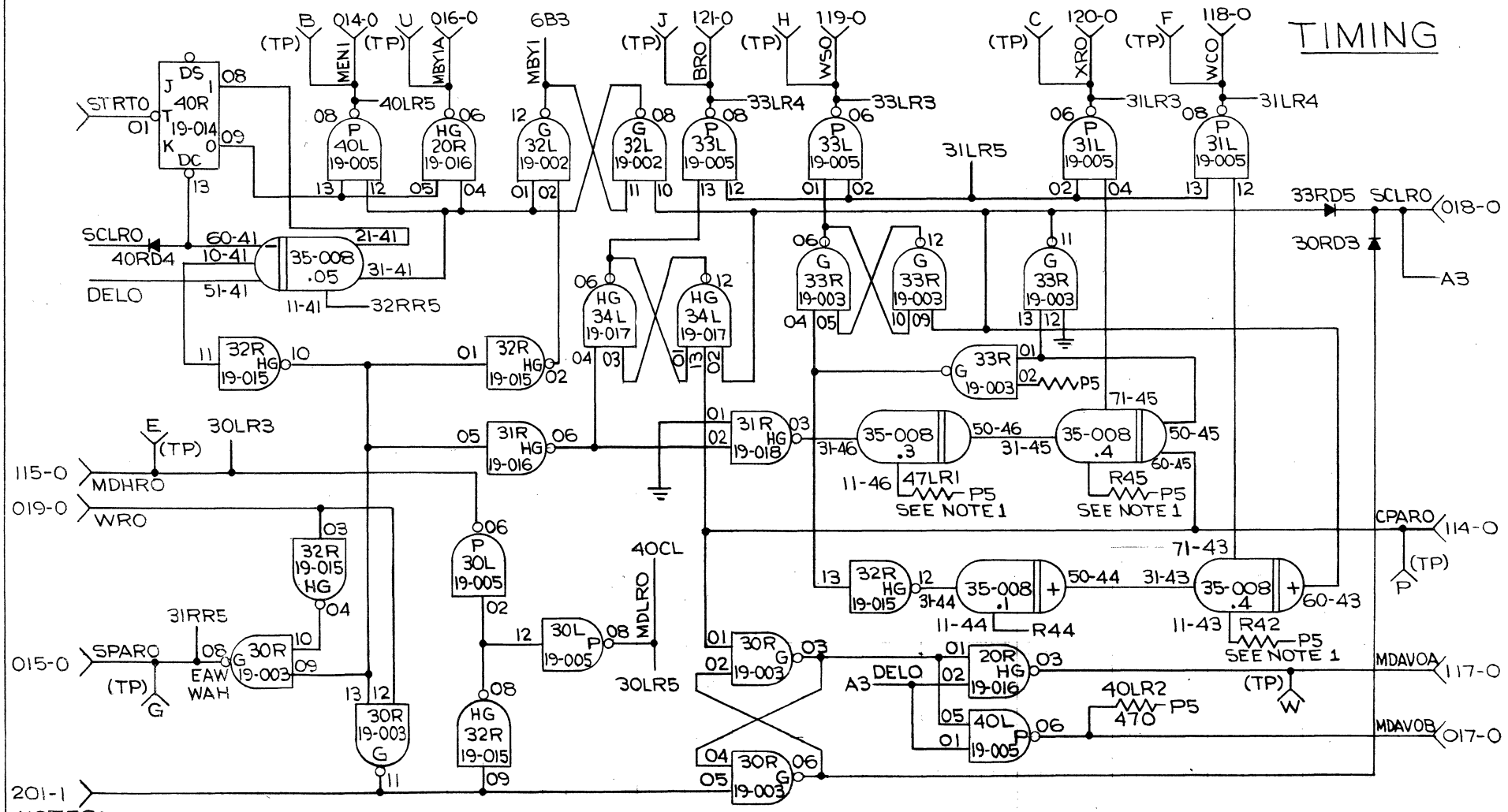
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
MEMORY STANDARD INTERFACE
FMF | FCF

DWG. NO. (FS28) 70B113000
CONT. ON SHEET 6 SH. NO. 5

TIMING



NOTES: 1. RESISTORS 47LR1, R42, & R45 ARE 6.8K, 10K & 10K FOR 35-096; & ARE 4.7K, 6.8K & 6.8K FOR 35-096 FOI RESPECTIVELY.

MADE BY	APPROVAL					DWG. NO.
E. Ellsworth JUL. 3, 1969	E. A. White June 26, 69	DES.	REV.	E		(FS28 70B113000
ISSUED JUL 18 1969		CHKR.				CONT ON SHEET 6 SH NO. 5

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:--

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
MEMORY STANDARD INTERFACE
FMF GE-PAC 30 | FCF

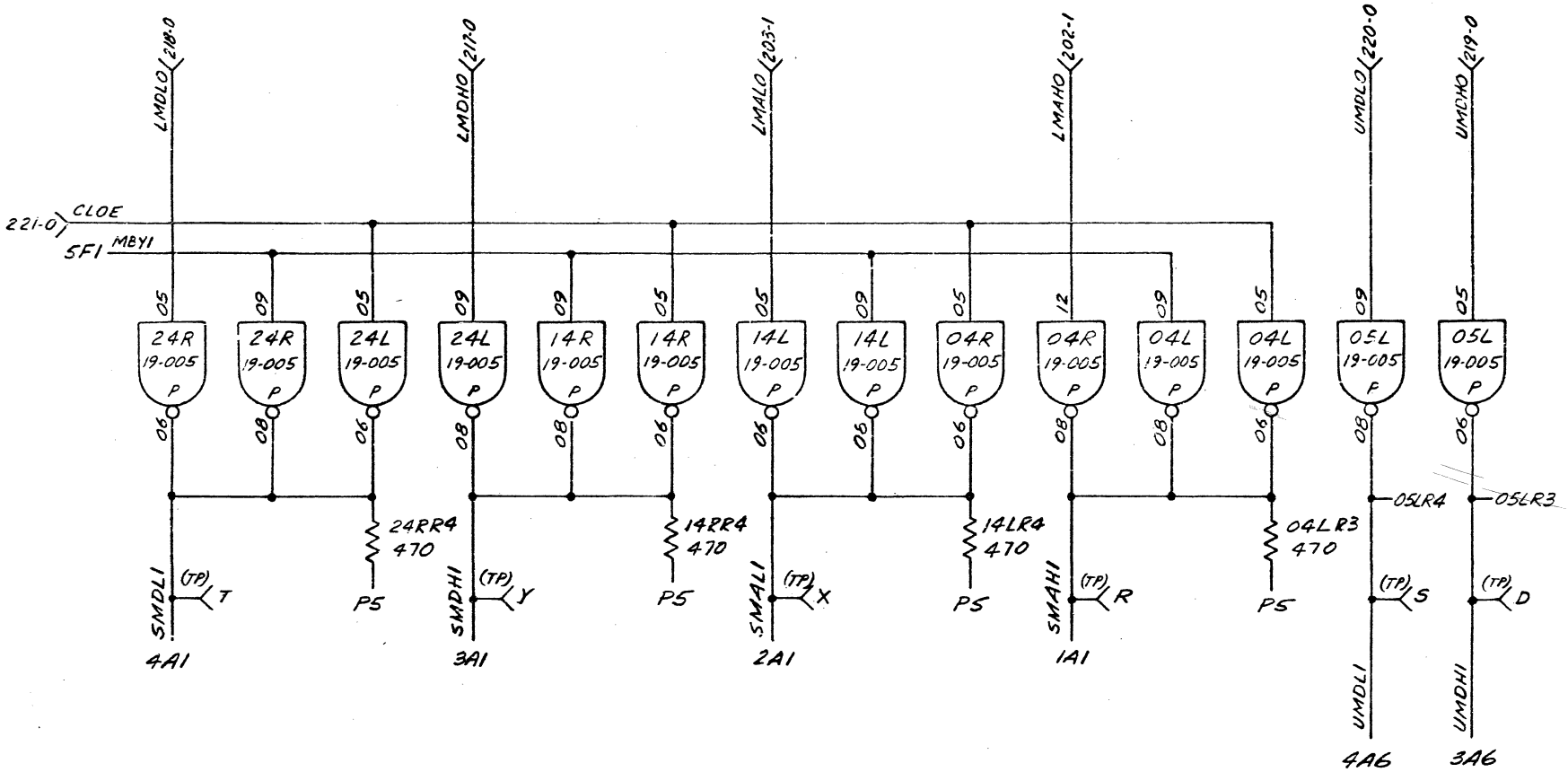
DWG. NO (FS28)
70B113000
CONT. ON SHEET 7 SH. NO. 6

A B C D E F G H J K L M N P R

1 2 3 4 5 6 7 8 9

3

LOAD CONTROL



MADE BY E. Ellsworth JUN 17, 1969
ISSUED JUL 18 1969

APPROVAL E. G. White June 26, 69
DES.
CHKR. DR
REV. E

DWG. NO (FS28)
70B113000
CONT ON SHEET 7 SH. NO. 6

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
MEMORY STANDARD INTERFACE
FMF GE-PAC 30 | FCF

DWG NO (FS28) 70B113000
CONT ON SHEET F SH NO 7

A B C D E F G H J K L M N P R

3

BACK PANEL MAP

	CONN POS		06																	
	MOTH. BD		(MSFC)																	
	VERT. POS		HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS		
		0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2
1	22		P5	GND																
	21																			
	20	MA15OA	MA14OA	S151																
2	19	MA13OA	MA12OA	S141																
	18	MA11OA	MA10OA	S131																
	17	MA09OA	MA08OA	S121																
	16	MA07OA	MA06OA	S111																
3	15	MA05OA	MA04OA	S101																
	14	MA03OA	MA02OA	S091																
	13	MA01OA	MA00OA	S081																
	12			S071																
/	11	MS15O	MS14O	S061																
	10	MS13O	MS12O	S051																
4	09	MS11O	MS10O	S041																
	08	MS09O	MS08O	S031																
	07	MS07O	MS06O	S021																
	06	MS05O	MS04O	S011																
	05	MS03O	MS02O	S001																
	04	MS01O	MS000																	
5	03			LMALO																
	02			LMAHO																
	01			CWRO																
	00		P5	GND																
	22		P5	GND																
	21	STRTO	BRO	CLOE																
6	20	HLFO	XRO	UMDLO																
	19	WRO	WSO	UMDHO																
	18	SCLRO	WCO	LMDLO																
	17	MDAVOB	MDAVOA	LMDHO																
	16	MBYIA		B150																
7	15	SPARO	MDHRO	B140																
	14	MENI	CPARO	B130																
	13		MDLRO	B120																
	12			B110																
0	11	MD15O	MD14O	B100																
	10	MD13O	MD12O	B090																
	09	MD11O	MD10O	B080																
8	08	MD09O	MD08O	B070																
	07	MD07O	MD06O	B060																
	06	MD05O	MD04O	B050																
	05	MD03O	MD02O	B040																
	04	MD01O	MD000	B030																
	03	SP5	SP4	B020																
	02	SP3	SP2	B010																
9	01	SP1	SP0	B000																
	00		P5	GND																

MADE BY C. Ellsworth JUN 17, 1969
ISSUED JUL 18 1969

APPROVAL E.A. White June 26, 69

DES. —
CHKR. QR
REV E

DWG. NO (FS28) 70B113000
CONT ON SHEET F SH NO. 7

GENERAL ELECTRIC

PROCESS COMPUTERS
PHOENIX ARIZONA

TITLE

FUNCTIONAL SCHEMATIC, TELETYPE INTERFACE

DRAWING NUMBER	CONT.	PAGE
70B113002	0A	0

FIRST MADE FOR
GE-PAC 30 PROJECT
(FS29)

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
B	ISSUED				

REISSUED

B Issued

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME

REISSUED

(FS29)

MADE BY	APPROVAL	REV.	DWG. NO.	CONT.	PAGE
C. Ellsworth JUN. 17, '69	[signature] J. A. White June 26, '69	B	70B113002	0A	0
ISSUED July 18, 1969			PRINTS TO: K7-08		

PCE 2981

DIST.	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING					GENERAL ELECTRIC	TITLE FUNCTIONAL SCHEMATIC	DWG NO (FS29)
	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES	PROCESS COMPUTER PHOENIX	TELETYPE INTERFACE	70B113002
		V	±	±	±	FMF GE-PAC 30 | FCF	CONT. ON SHEET |	SH NO 0A

SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
SHEET INDEX SUPPORTING INFORMATION	0A	/																			
DAL RCVRS & ADDRESS CIRCUIT	1	/																			
DAL BUS DRIVERS & ACK ADDRESS GATES	2	/																			
CONT. LINE RCVRS & GATES ATN/EBL CKT	3	/																			
DATA SHIFT REGISTER	4	/																			
TIMER & EOC GATES	5	/																			
CONTROL CIRCUITS	6	/																			
TTY COUPLER CIRCUITS	7	/																			
TTY POWER CONTROL	8	/																			
STATUS & DRL GATES	9	/																			
CMD GATES & FLOPS, BSY LOGIC	10	/																			
BACK PANEL MAP	11	/																			
BLOCK DIAGRAM	12	/																			

SUPPORTING INFORMATION

CATEGORY	PART NO.
MOTHER BOARD TTY INTERFACE:	
WITHOUT PWR CONTROL	32-062R01F01
WITH PWR CONTROL	32-062R01F02

SHEET INDEX NOTES:

1. CHANGES ON THIS DRAWING SHALL REQUIRE ONLY THE REISSUE OF SHEETS AFFECTED.
2. THE ISSUE OF THIS SHEET SHALL DETERMINE THE LATEST ISSUE OF THIS DRAWING.

MADE BY	APPROVAL		REV.		DWG. NO. (FS29)
C. Ellsworth JUN. 17, '69	E.A. White June 26, 69	DES.	B		70B113002
ISSUED JUL 18 1969		CHKR. DR			CONT ON SHEET | SH NO 0A

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

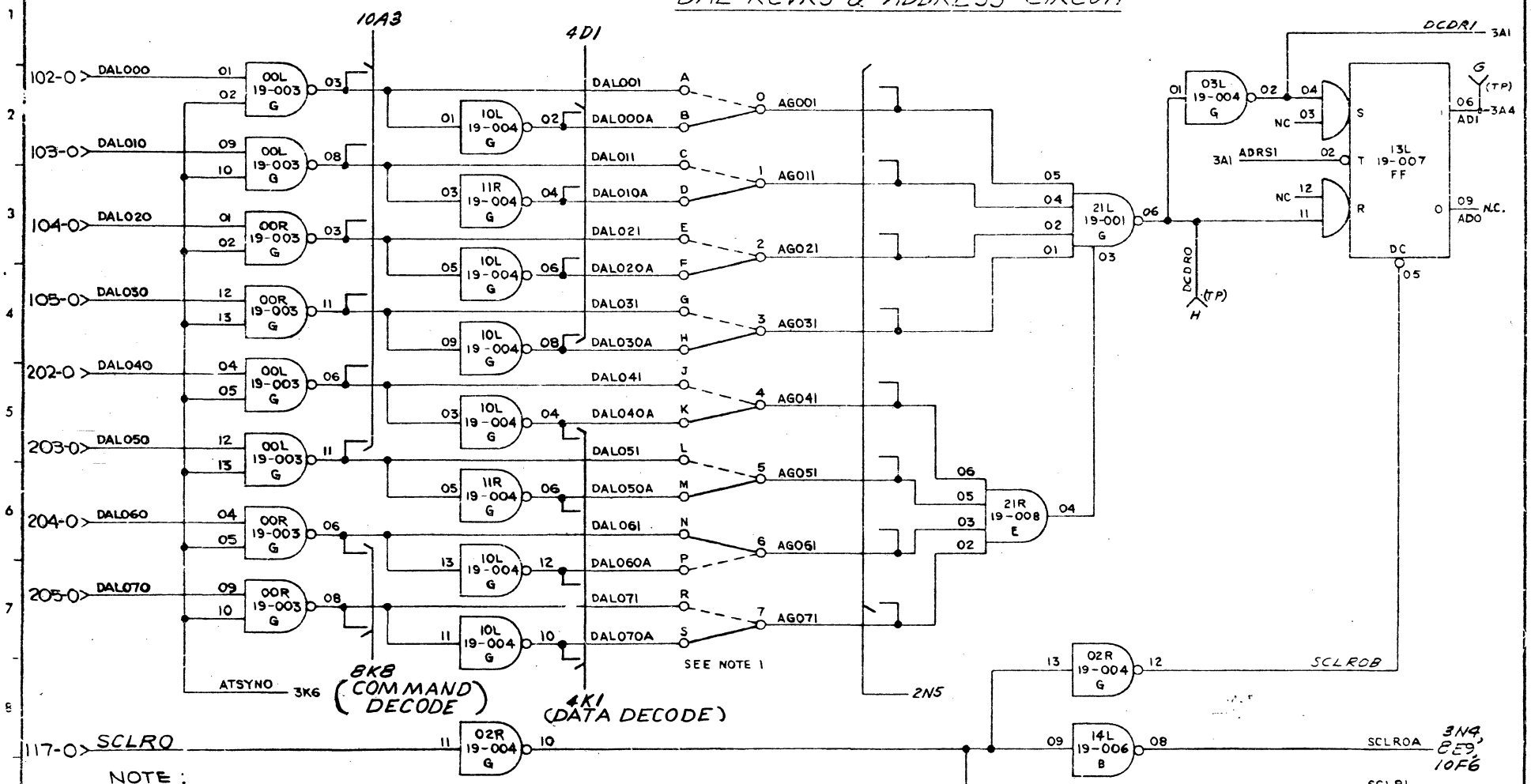
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
TELETYPE INTERFACE
FMF GE-PAC 30 | FCF

DWG NO (FS29)
70B113002
CONT ON SHEET 2 SH NO 1

DAL RCVRS & ADDRESS CIRCUIT



NOTE:
1. STRAP FOR ϕ2 ADDRESS NORMALLY.

MADE BY C. Ellsworth JUN. 17, '69
ISSUED JUL 18 1969

APPROVAL E.A. White June 26, 69

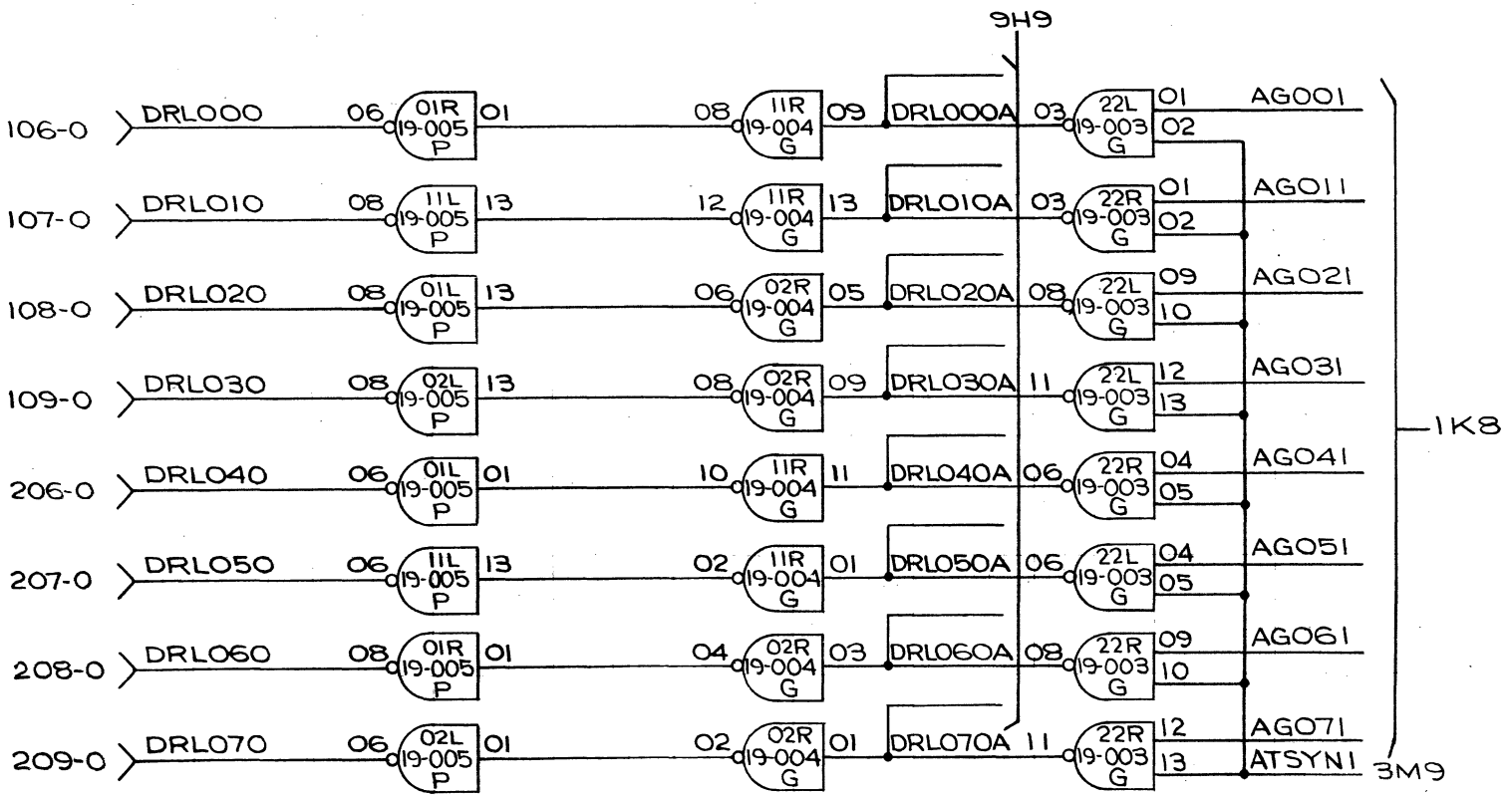
DES.
CHKR. OK

REV. B

DWG NO (FS29)
70B113002
CONT ON SHEET 2 SH NO 1

DIST.	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—					GENERAL ELECTRIC	TITLE FUNCTIONAL SCHEMATIC	DWG. NO. (FS29)
	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES	PROCESS COMPUTER PHOENIX	TELETYPE INTERFACE	70B113002
		✓	±	±	±	FMF GE-PAC 30 1 FCF	CONT. ON SHEET 3	SH. NO. 2

DAL BUS DRIVERS & ACK ADDRESS GATES



MADE BY C.E.Ellsworth JUL.1,1969	APPROVAL	DES.		REV.	B								DWG. NO. (FS29) 70B113002
ISSUED JUL 18 1969		CHKR.											CONT ON SHEET 3 SH NO. 2

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±
SURFACES: √

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
TELETYPE INTERFACE
FMF GE-PAC 30 1 FCF

DWG. NO. (FS29) 70B113002
CONT. ON SHEET 4 SH. NO. 3

CONTROL LINE RCVRS & GATES
ATN/EBL CIRCUIT

1R1 DCDR1
1M3 ADRS1
03LC1 470PF
110-0 ADRS0
210-0 CMDO
111-0 DAO
113-0 SRO
112-0 DRO
1R2 ADI
6R3 TMGO
115-0 SYNO
215-0 ATNO
114-0 RACKO
214-0 TACKO

03L 19-004 G
03R 19-003 G
04R 19-006 B
21R 19-008 E
21L 19-001 G
12L 19-005 P
23L 19-005 P
23R 19-003 G
10R 19-006 B
13R 19-003 G

CMGO 10A7
DAGO 4P1, 5N5, 6A5
SRGO 9A1
DRGO 9M1
ATSYNO 1C8
ASYNO
SYNI
11LC5 470PF (TP) C
12LC2 470PF
ATN1
23RR2
23RR5
23LR5
ATSYN1 2N7
12RC2 100PF
12RC6 BSY1 10R5 470PF
12RR5
1R8 SCLR0A
(TP) F
(TP) J
EBL0
EBL1
10G2
N.C.

12R 19-007 FF DS
DC R S T

STILL CHANGING SOFTWARE
BY PASSES TV INTERFACE

MADE BY C. Ellsworth JUL. 1, 1969
ISSUED JUL 18 1969
APPROVAL
DES. CHKR. REV. B

DWG. NO. (FS29) 70B113002
CONT ON SHEET 4 SH. NO. 3

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --

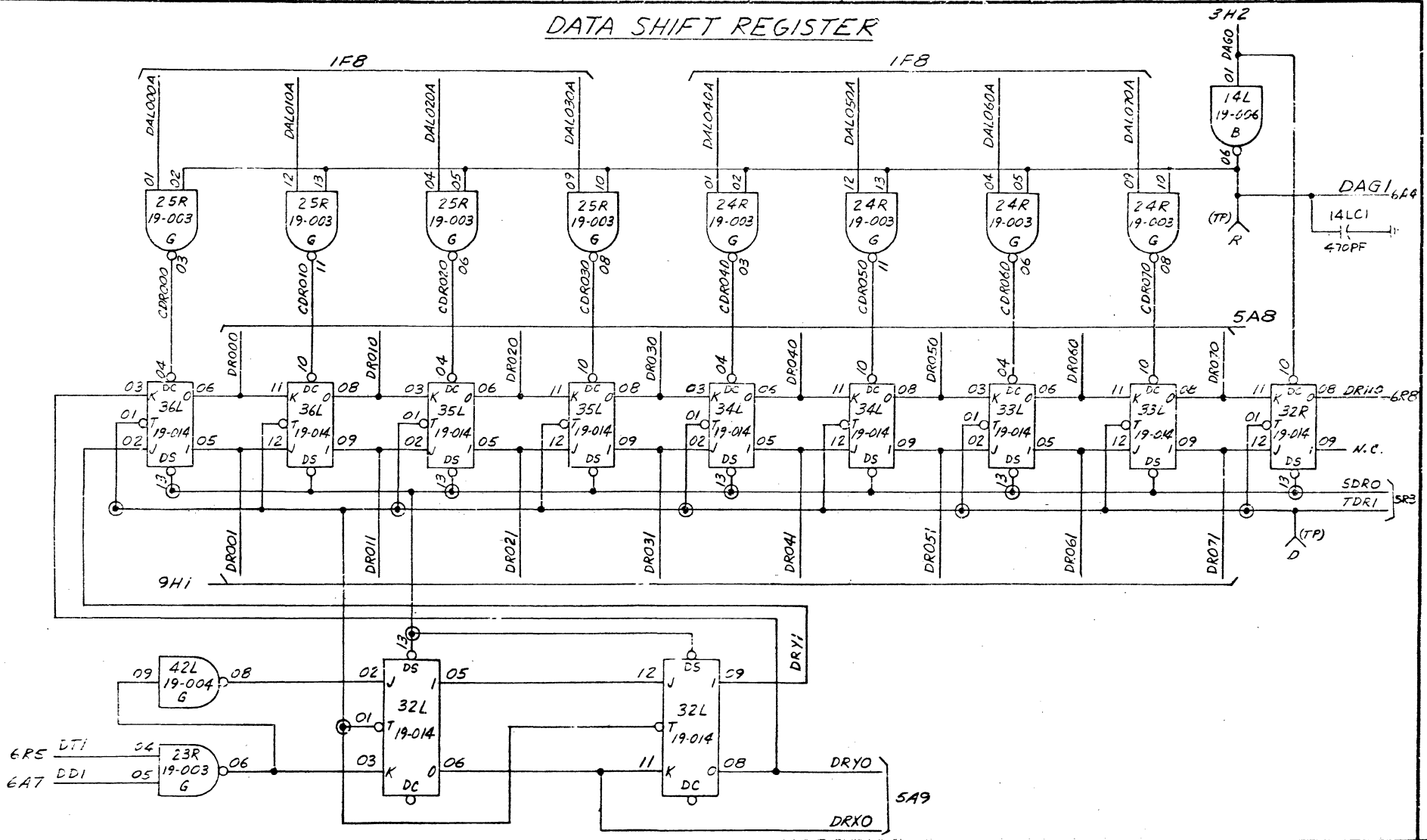
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
TELETYPE INTERFACE
FMF GE-PAC 30 1 FCF

DWG NO (FS29) 70B113002
CONT. ON SHEET 5 SH NO 4

DATA SHIFT REGISTER



MADE BY E. Ellsworth JUN. 17, 69
ISSUED JUL 18 1969

APPROVAL E. A White June 26, 69

DES.
CHKR. DR

REV. B

DWG. NO. (FS29) 70B113002
CONT ON SHEET 5 SH NO. 4

DIST.

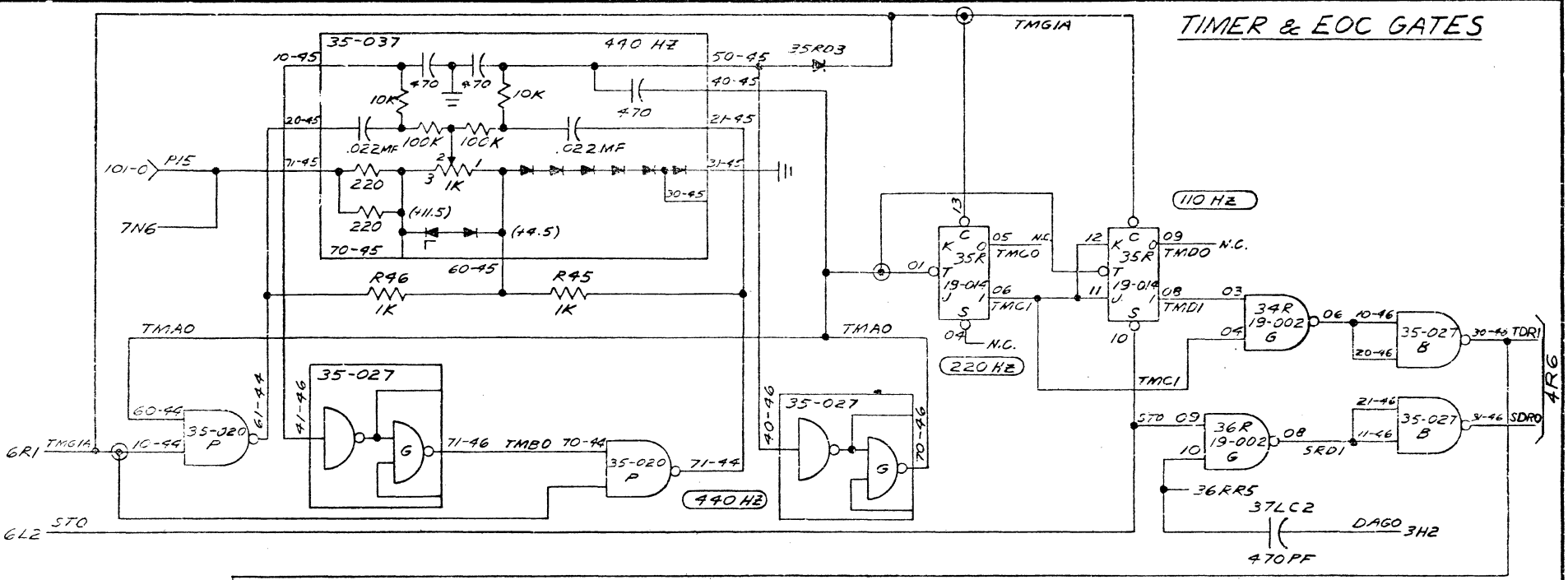
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --
APPLIED PRACTICES | SURFACES | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±
SURFACES: √

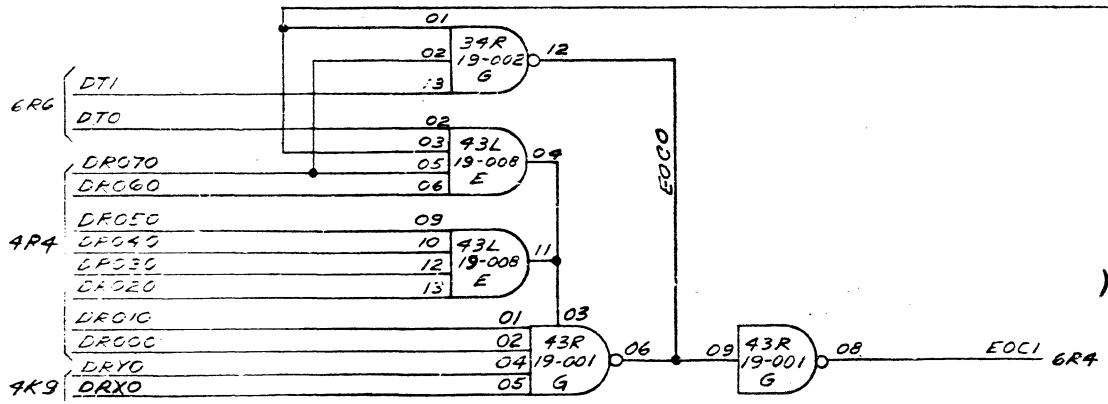
GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL MODULE
TELETYPE INTERFACE
FMF GE-PAC 30 | FCF

DWG. NO (FS29) 70B113002
CONT. ON SHEET 6 SH NO. 5

TIMER & EOC GATES





MADE BY E Ellsworth JUN. 17, 69
ISSUED JUL 18 1969
APPROVAL E. G White June 26, 69
DES.
CHKR. DR
REV. B

DWG. NO. (FS29) 70B113002
CONT ON SHEET 6 SH NO. 5

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:
APPLIED PRACTICES | SURFACES: V | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
TELETYPE INTERFACE
FMF GE-PAC 30 | FCF

DWG. NO. (FS29)
70B113002
CONT. ON SHEET 7 SH NO. 6

CONTROL CIRCUITS

TMGO
ASTO
ASTI
STO
TMGIA
35RR6
TMGO (TP) P
TIMING FF
TMGI
TMGO
CTMGO
EOCI
RDYI
SRDYO
R4 EOCI
READY FF
4R3 DAGI
RDYO
DDOA
BRKO
BRKI
DEVICE TRANSMIT FF
3H2 DAGO
DAGIA
DTI
DTO
DDOA
7N1
4A9 DDI
DDO
7M1
1R9 SCLRI
CDTO
9M4 DRGI
7R4 TRNSO
BITS TO TTY
TRNSI
DRINO
PS
BLKDTO

26L 19-002 G	42L 19-004 G
26R 19-004 G	15R 19-003 G
17R 19-006 B	35-020 P
25L 19-014	24L 19-002 G

26RC2 470PF

MADE BY C. Ellsworth JUN. 17, '69
ISSUED JUL 18 1969
APPROVAL E.G White June 26, 69
DES.
CHKR. OR
REV. B

DWG. NO. (FS29)
70B113002
CONT ON SHEET 7 SH NO. 6

DIST.

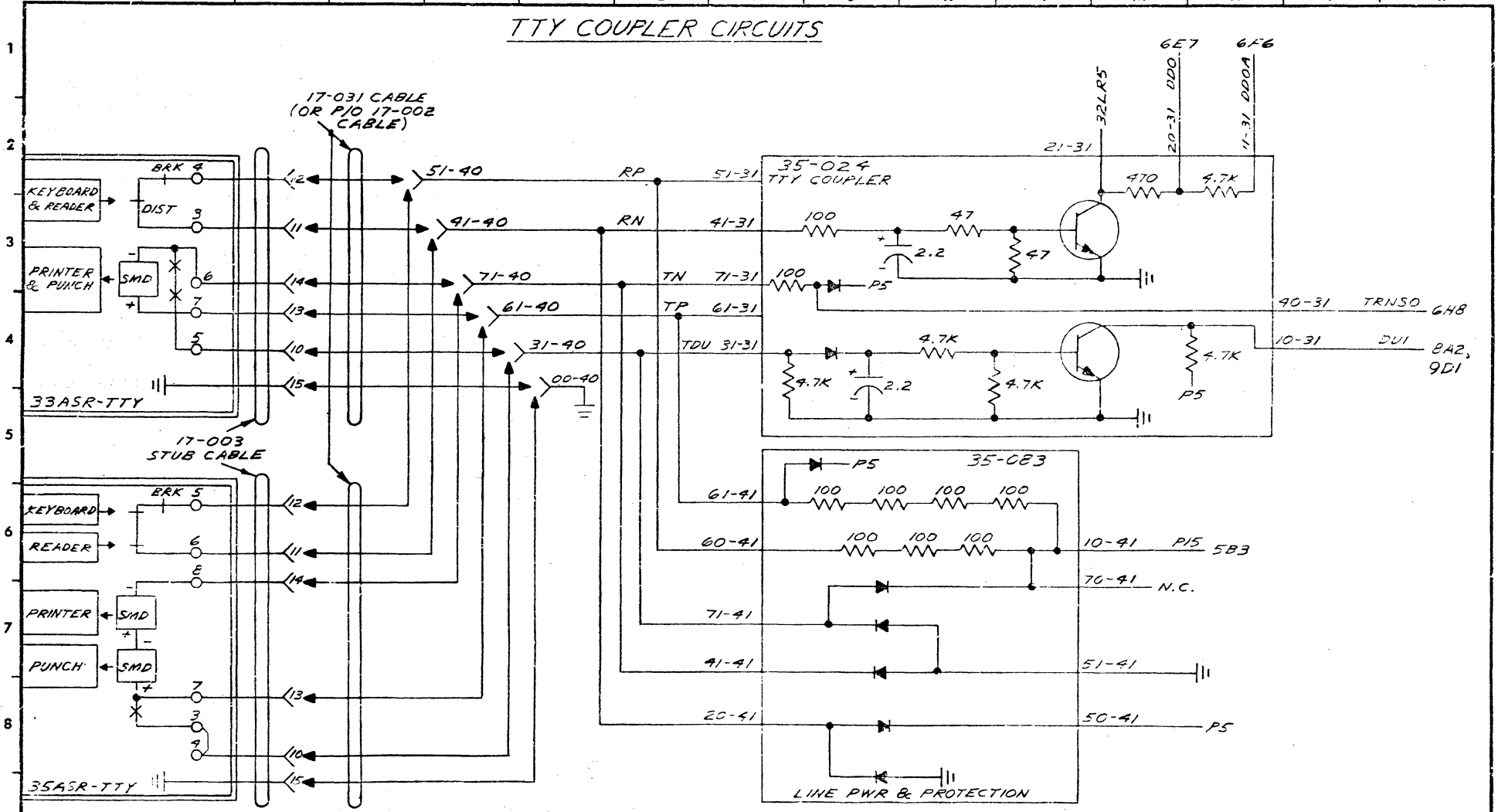
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --
APPLIED PRACTICES | SURFACES | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS | DECIMALS | ANGLES
SURFACES: √ | FRACTIONS: ± | DECIMALS: ± | ANGLES: ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
TELETYPE INTERFACE
FMF GE-PAC 30 | FCF

DWG NO (FS 29)
70B113002
CONT ON SHEET 8 | SH NO 7

TTY COUPLER CIRCUITS



MADE BY G. Ellsworth JUN 17, 69
ISSUED JUL 18 1969

APPROVAL E. a. White June 26, 69

DES.
CHKR. DR

REV. B

DWG. NO (FS 29)
70B113002
CONT ON SHEET 8 | SH NO. 7

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±
SURFACES: √

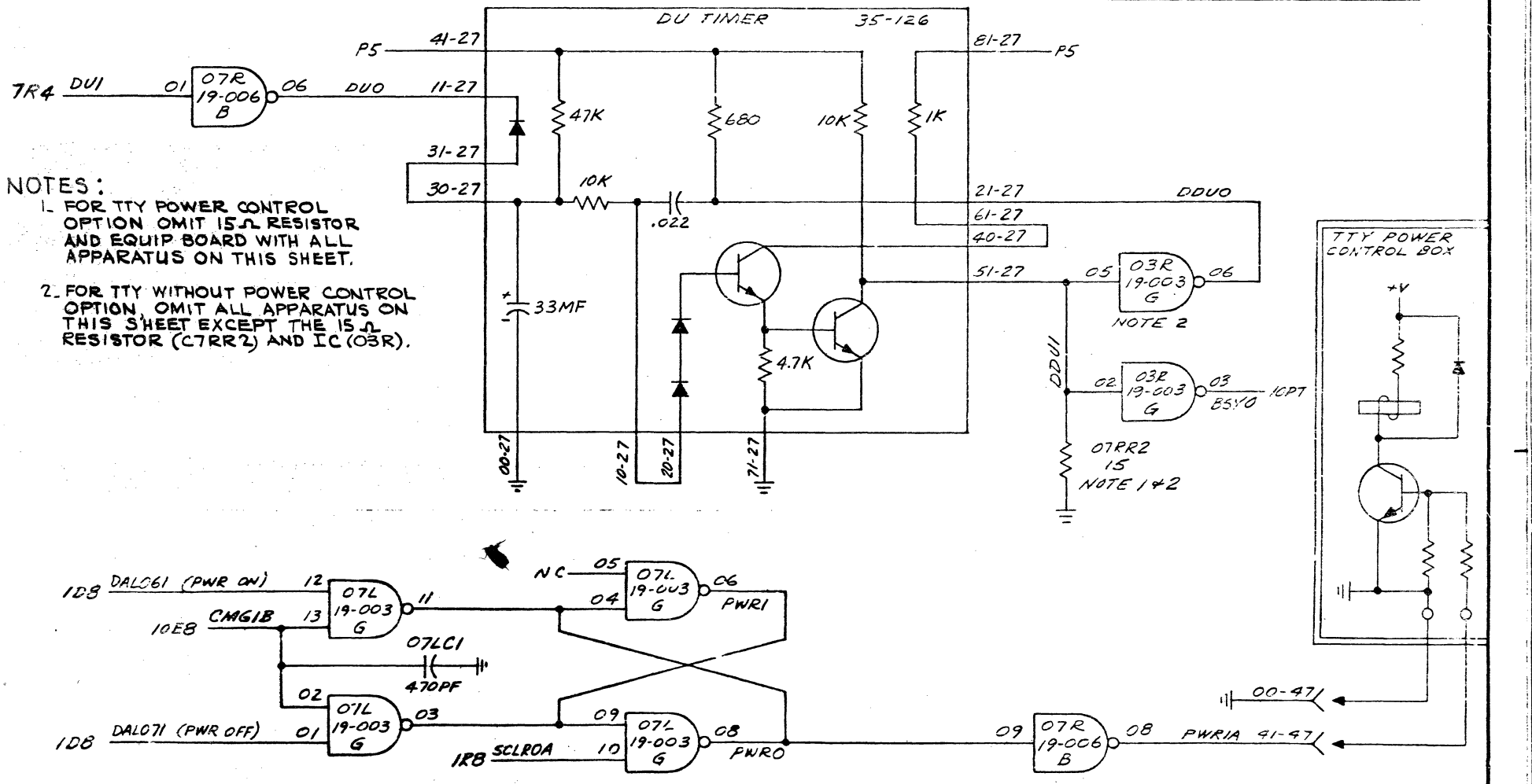
GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
TELETYPE INTERFACE
FMF GE-PAC 30 | FCF

DWG. NO. (FS 29)
70B113002
CONT. ON SHEET 9 SH NO 8

A B C D E F G H J K L M N P R

TTY POWER CONTROL



NOTES:
1. FOR TTY POWER CONTROL OPTION OMIT 15Ω RESISTOR AND EQUIP BOARD WITH ALL APPARATUS ON THIS SHEET.
2. FOR TTY WITHOUT POWER CONTROL OPTION, OMIT ALL APPARATUS ON THIS SHEET EXCEPT THE 15Ω RESISTOR (C7RR2) AND IC (03R).

MADE BY	APPROVAL				DWG. NO.
E. Ellsworth JAN 17, '69	E. A. White June 26, 69	DES.		B	70B113002
ISSUED JUL 18 1969		CHKR. OR			CONT ON SHEET 9 SH NO. 8

DIST.

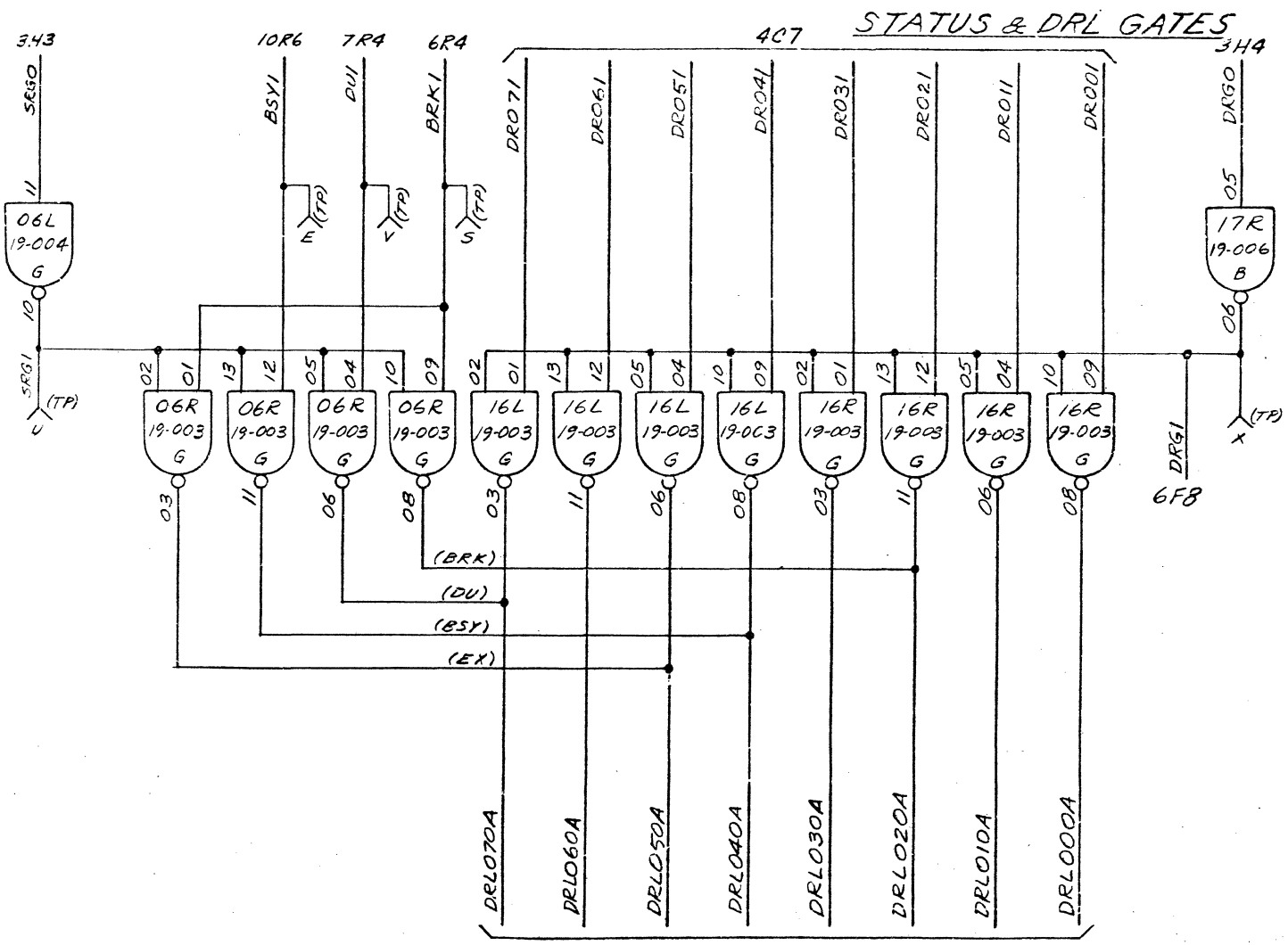
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
TELETYPE INTERFACE
FMF GE-PAC 30 | FCF

DWG NO (FS29) 70B113002
CONT. ON SHEET 10 SH NO 9

STATUS & DRL GATES



TP	NAME	SH
Y	READ 1	10
X	DRG 1	9
W	BLK 1	10
V	DU 1	9
U	SRG 1	9
T		
S	BRK 1	9
R	DAG 1	4
P	TMGO	6
N		
M		
K		
J	ATN 1	3
H	DCDRO	1
G	AD 1	1
F	EBL 1	3
E	BSY 1	9
D	TDR 1	4
C	SYN 1	3
B		
A	GND	

CMD	BIT	STATUS
DISABLE	0	
ENABLE	1	
UNBLOCK	2	BRK
BLOCK	3	
WRITE	4	BSY
READ	5	EX
PWR-ON	6	
PWR-OFF	7	DU

MADE BY E Ellsworth JUN 17, '69
ISSUED JUL 18 1969
APPROVAL E.G. White June 26, 69
DES.
CHKR. DR
REV. B

DWG. NO (FS29) 70B113002
CONT ON SHEET 10 SH NO 9

DIST.

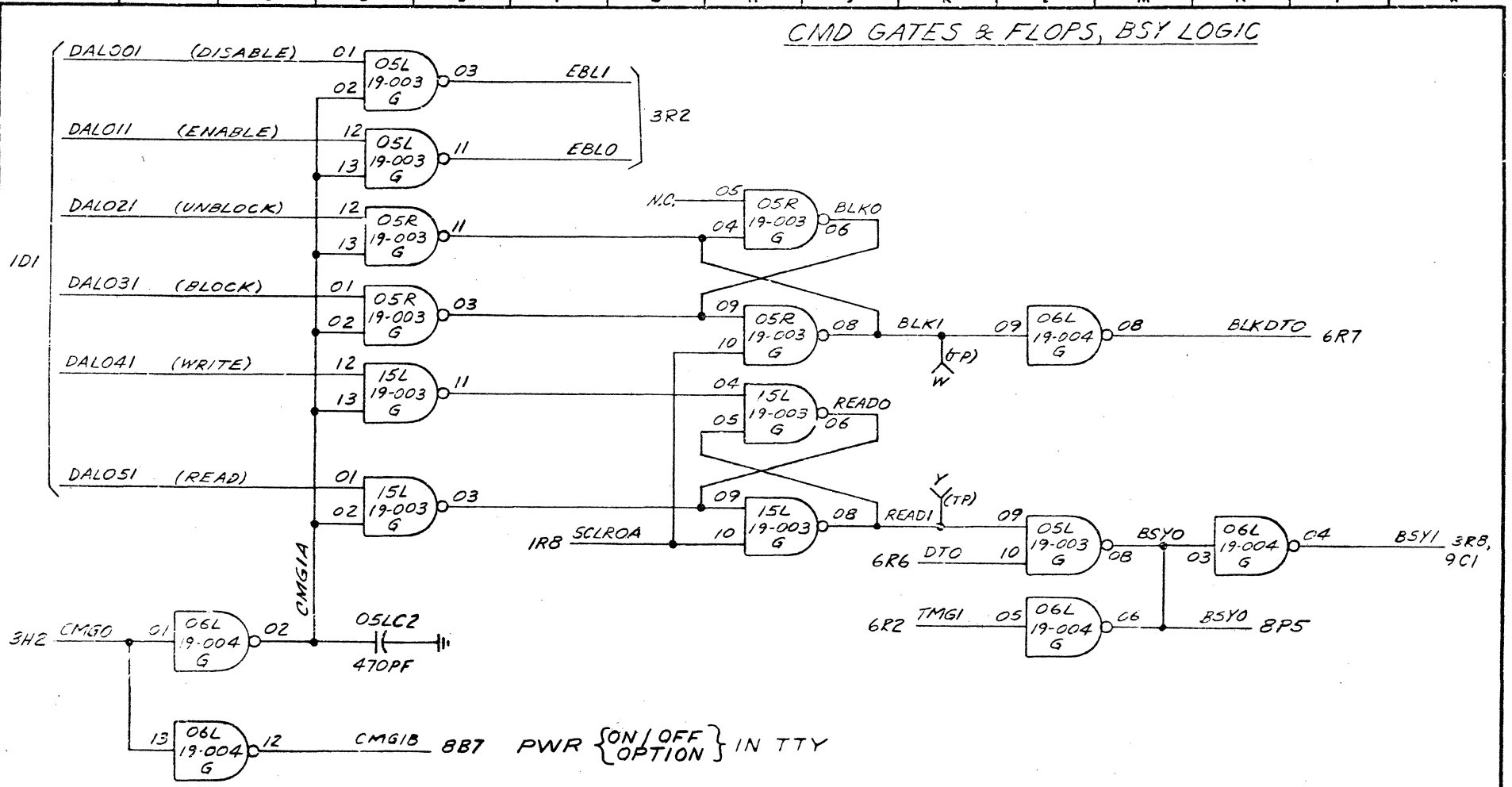
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:
APPLIED PRACTICES | SURFACES: V | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
TELETYPE INTERFACE
FMF GE-PAC 30 1 FCF

DWG NO (FS29) 70B113002
CONT ON SHEET 11 SH NO 10

CMD GATES & FLOPS, BSY LOGIC



MADE BY	APPROVAL				
E. Ellsworth JAN 17,'69	E.G. White June 26, 69	DES.		B	DWG. NO. (FS29) 70B113002
ISSUED JUL 18 1969		CHKR. OR	REV		CONT ON SHEET 11 SH NO. 10

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
TELETYPE INTERFACE
FMF GE-PAC 30 | FCF

DWG NO (FS29) 70C113002
CONT ON SHEET 12 SH NO 11

BACK PANEL MAP

CONN POS	21			23			25											
MOTH. BD	DSP OR TTY			TTY			TTY											
VERT. POS	HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS		
	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2
22																		
21																		
20																		
19																		
18																		
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08																		
07																		
06																		
05																		
04																		
03																		
02																		
01																		
00																		
22		P5	GND		P5	GND		P5	GND									
21																		
20			ENBCO															
19		SNGLO	ESNCO															
18		CATNO	ESNDO															
17		SCLRO			SCLRO			SCLRO										
16																		
15		SYNO	ATNO		SYNO	ATNO		SYNO	ATNO									
14		ACKA000	ACKA010		ACKA010	ACKA020		ACKA020	ACKA030									
13		SRO	CLO70		SRO	CLO70		SRO	CLO70									
12		DRO	CLO60		DRO	CLO60		DRO	CLO60									
11		DAO			DAO			DAO										
10		ADRSO	CMDO		ADRSO	CMDO		ADRSO	CMDO									
09		DRL030	DRL070		DRL030	DRL070		DRL030	DRL070									
08		DRL020	DRL060		DRL020	DRL060		DRL020	DRL060									
07		DRL010	DRL050		DRL010	DRL050		DRL010	DRL050									
06		DRL000	DRL040		DRL000	DRL040		DRL000	DRL040									
05		DAL030	DAL070		DAL030	DAL070		DAL030	DAL070									
04		DAL020	DAL060		DAL020	DAL060		DAL020	DAL060									
03		DAL010	DAL050		DAL010	DAL050		DAL010	DAL050									
02		DAL000	DAL040		DAL000	DAL040		DAL000	DAL040									
01		P15	N15		P15	N15		P15	N15									
00		P5	GND		P5	GND		P5	GND									

MADE BY G. Ellsworth JUN. 17, '69
ISSUED JUL 18 1969

APPROVAL E. G. White June 26, 69

DES.
CHKR. DR

REV. B

DWG. NO (FS29) 70C113002
CONT ON SHEET 12 SH NO. 11

DIST.

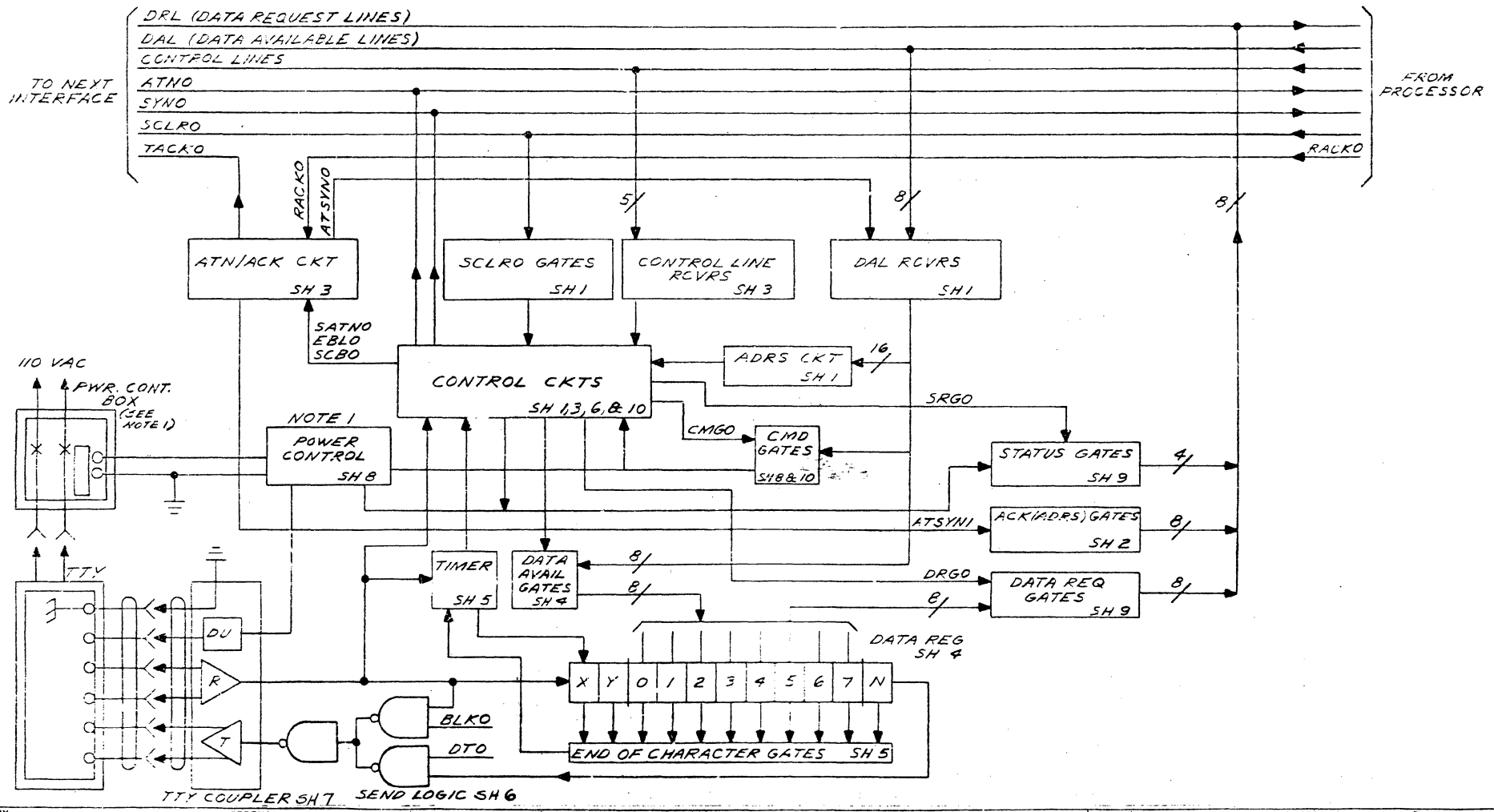
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING –
APPLIED PRACTICES | SURFACES | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±
SURFACES: √

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
TELETYPE INTERFACE
FMF GE-PAC 30 | FCF

DWG NO (FS29) 70B113002
CONT. ON SHEET F SH NO 12

BLOCK DIAGRAM



MADE BY C. Ellsworth JUN. 17, '69
ISSUED JUL 18 1968
APPROVAL E. A. White June 26, 69
DES.
CHKR. DR
REV. B

DWG. NO (FS29) 70B113002
CONT ON SHEET F SH NO. 12

GENERAL ELECTRIC

PROCESS COMPUTERS
PHOENIX ARIZONA

TITLE

FUNCTIONAL SCHEMATIC, DISPLAY CONTROLLER

DRAWING NUMBER 70B113003 | CONT. 0A | PAGE 0

FIRST MADE FOR GE-PAC 30 PROJECT

(FS31)

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
C	ISSUED				

REISSUED

Released

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME

REISSUED

(FS31)

MADE BY	APPROVAL	REV.		DWG. NO.	CONT.	PAGE
E. Ellsworth JUN 17, 69	E. A. White June 25, 69	C		70B113003	0A	0
ISSUED July 18, 1969				PRINTS TO: K7-08		

PCE 2981

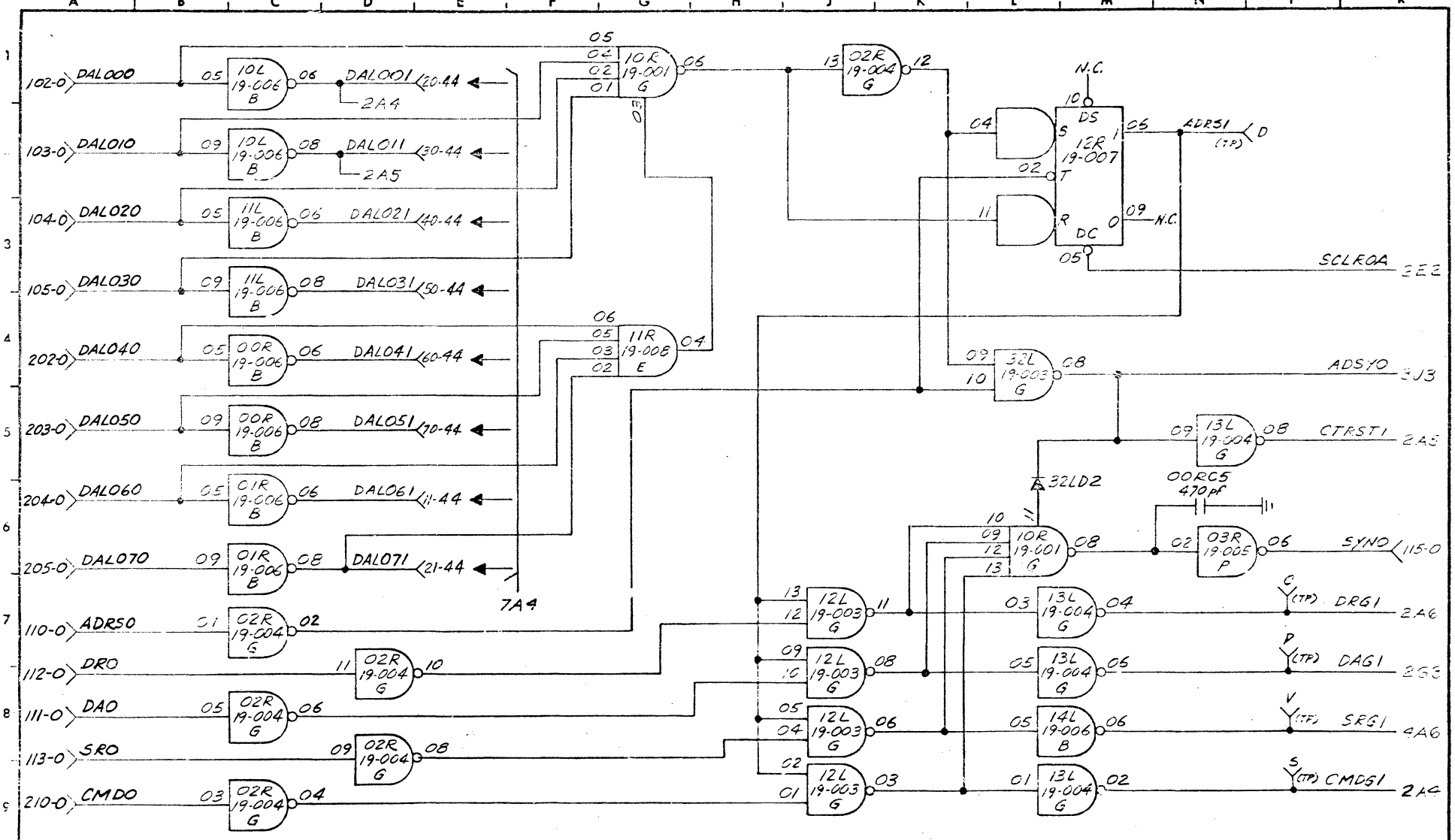
DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING :-
APPLIED PRACTICES | SURFACES √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
DISPLAY CONTROLLER
FMF GE-PAC 30

DWG NO (FS31)
70B113003
CONT ON SHEET 2 SH NO 1



MADE BY E. Ellsworth JUN.17.'69
DATE JUL 13 1969
APPROVAL S. G. White June 25, 69
DES.
CHKR. OR
REV. B

DWG. NO (FS31)
70B113003
CONT ON SHEET 2 SH NO 1

DIST.

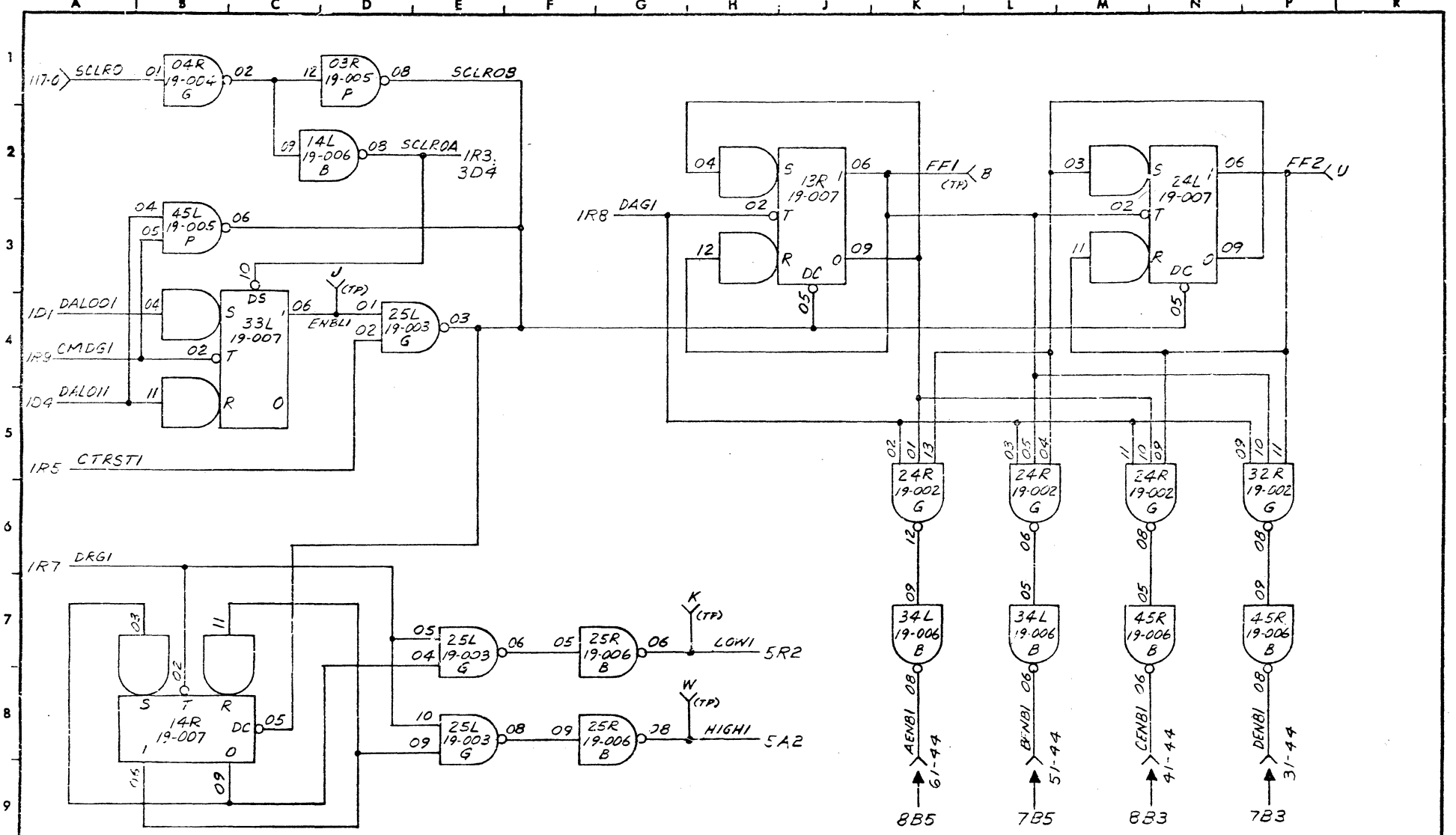
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING –

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS		
		FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
DISPLAY CONTROLLER
FAC GE-PAC 30 FSC

DWG NO (FS 31) 70B113003
CONT ON SHEET 3 SH NO 2



MADE BY	APPROVAL	DES.		REV.								
E. Ellsworth JUN.17,69	E. A. White June 25, 69	CHKR.	AR		B							
ISSUED JUL 18 1969												

DWG. NO. (FS 31) 70B113003
CONT ON SHEET 3 SH NO. 2

DIST.

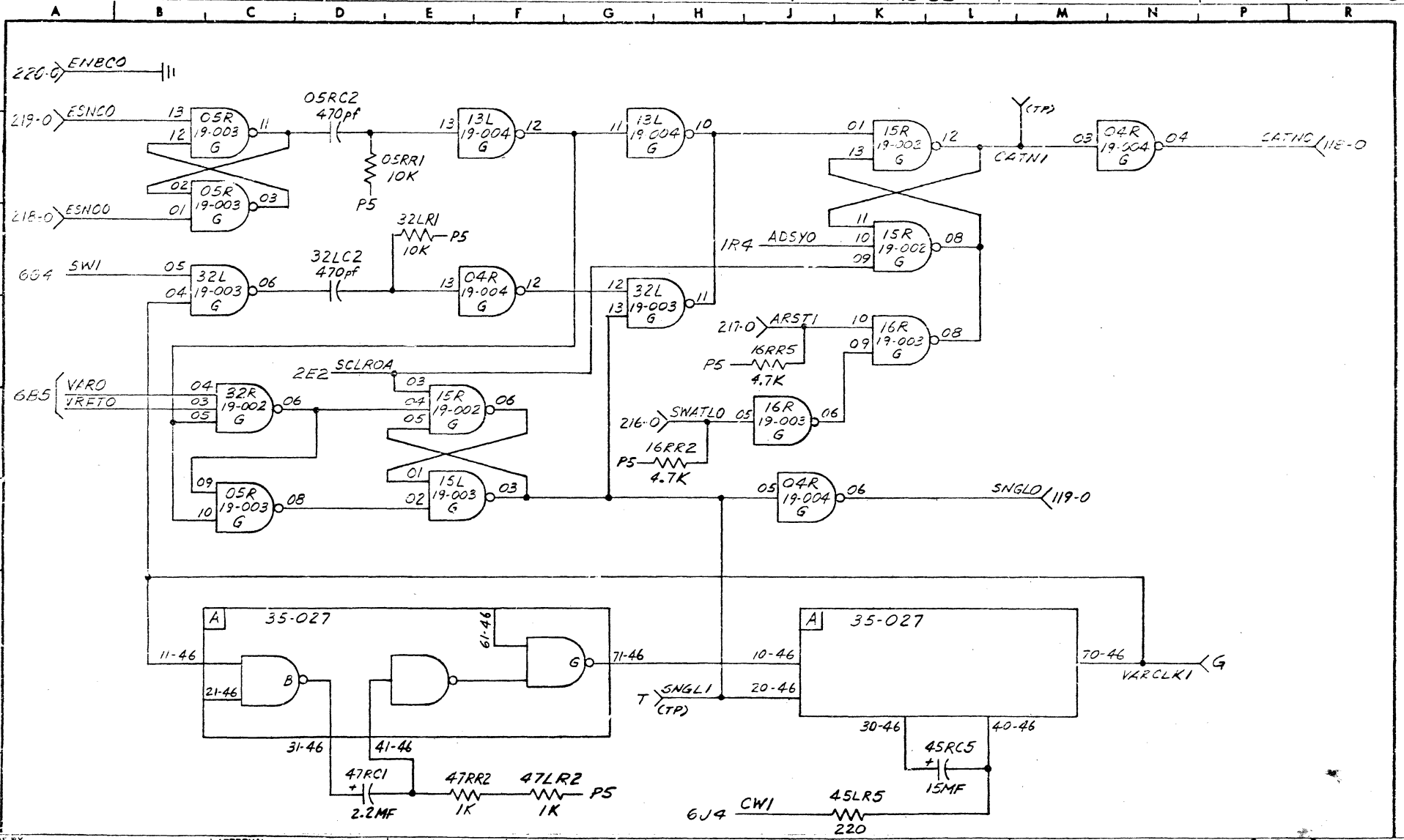
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
DISPLAY CONTROLLER
FMF GE-PAC 30 | FCF

DWG NO (FS31) 70B113003
CONT ON SHEET 4 SH NO 3



MADE BY	APPROVAL						DWG. NO (FS31)
C. Ellsworth JUN.17, 69	E. A. White June 25, 69	DES.		REV.	B		70B113003
ISSUED JUL 18 1969		CHKR.	DR				CONT ON SHEET 4 SH NO 3

DIST.

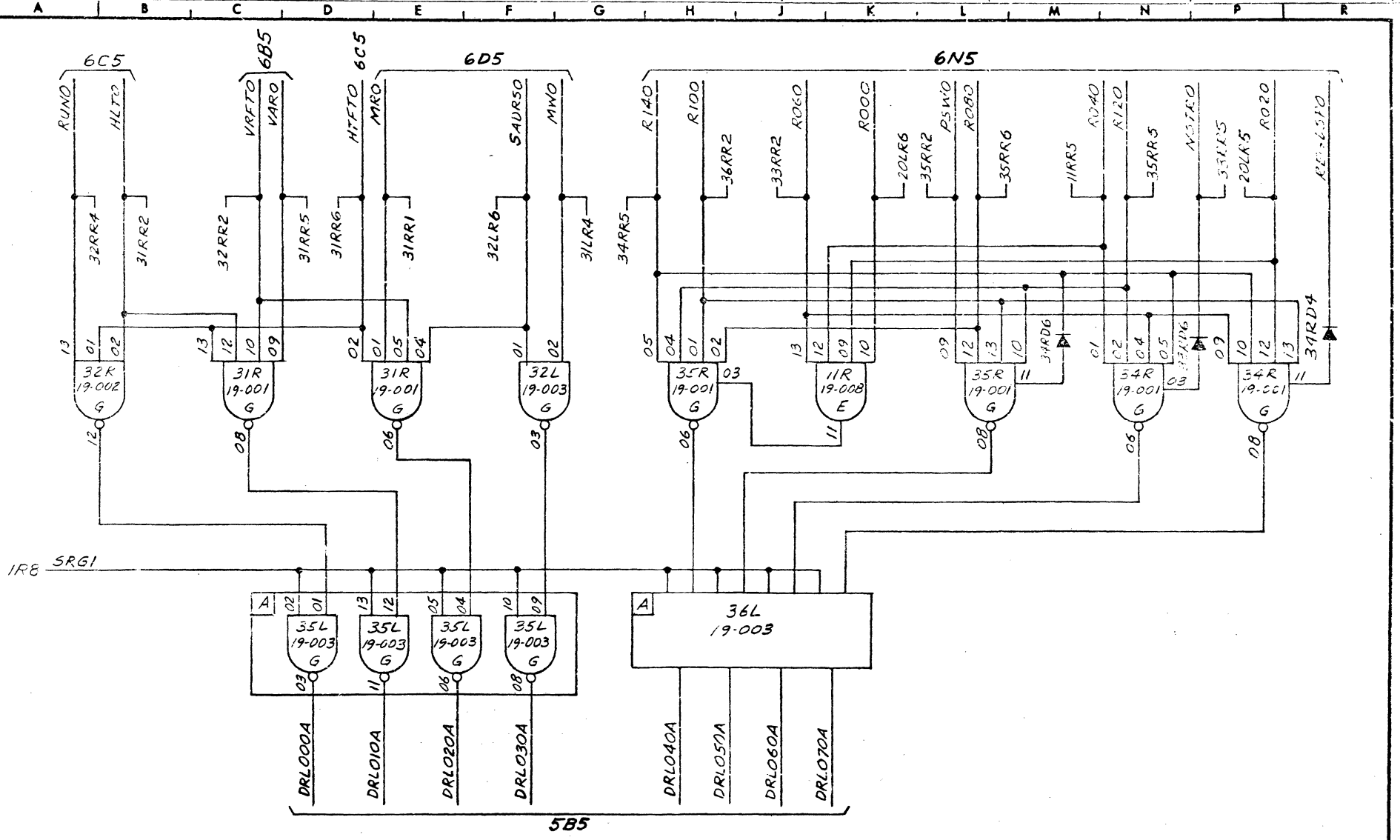
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
DISPLAY CONTROLLER
FMF GE-PAC 30 | FCF

DWG. NO (FS31)
70B113003
CONT. ON SHEET 5 SH NO 4



MADE BY C. Ellsworth JUN.17,'69
ISSUED JUL 18 1969

APPROVAL E. A. White June 25, 69
DES.
CHKR. DR
REV. B

DWG. NO. (FS31)
70B113003
CONT ON SHEET 5 SH NO. 4

DIST.

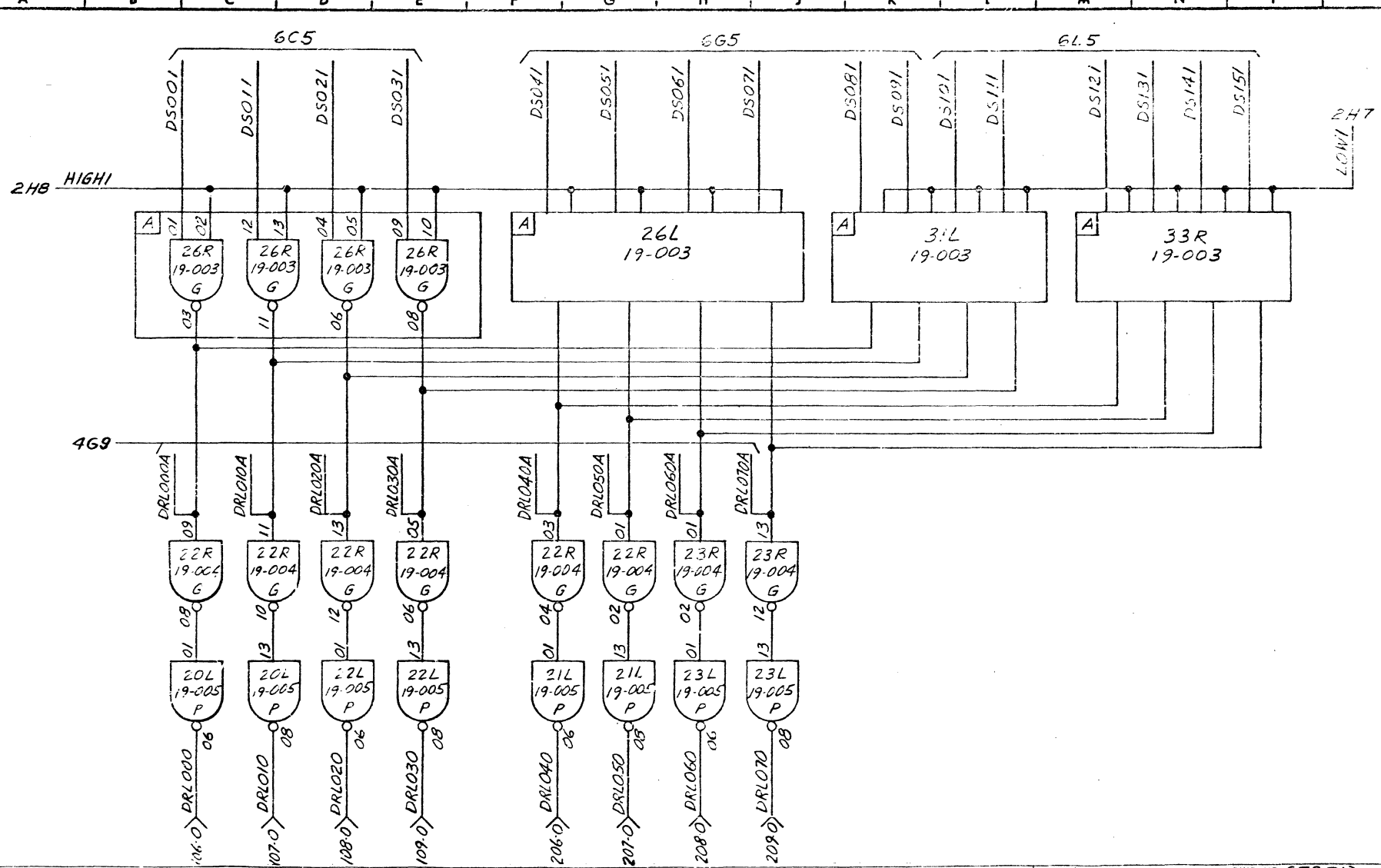
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
DISPLAY CONTROLLER
FMF GE-PAC 30 | FCF

DWG NO (FS31)
70B113003
CONT. ON SHEET 6 SH NO 5



MADE BY E. Ellsworth JUN.17,69
JUL 18 1969

APPROVAL E. A. White June 25, 69

DES.
CHKR. CR

REV. B

DWG. NO (FS31)
70B113003
CONT ON SHEET 6 SH NO. 5

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
DISPLAY CONTROLLER
FMF GE-PAC 30 1 FCF

DWG NO (FS 31) 70B113003
CONT. ON SHEET 7 SH NO 6

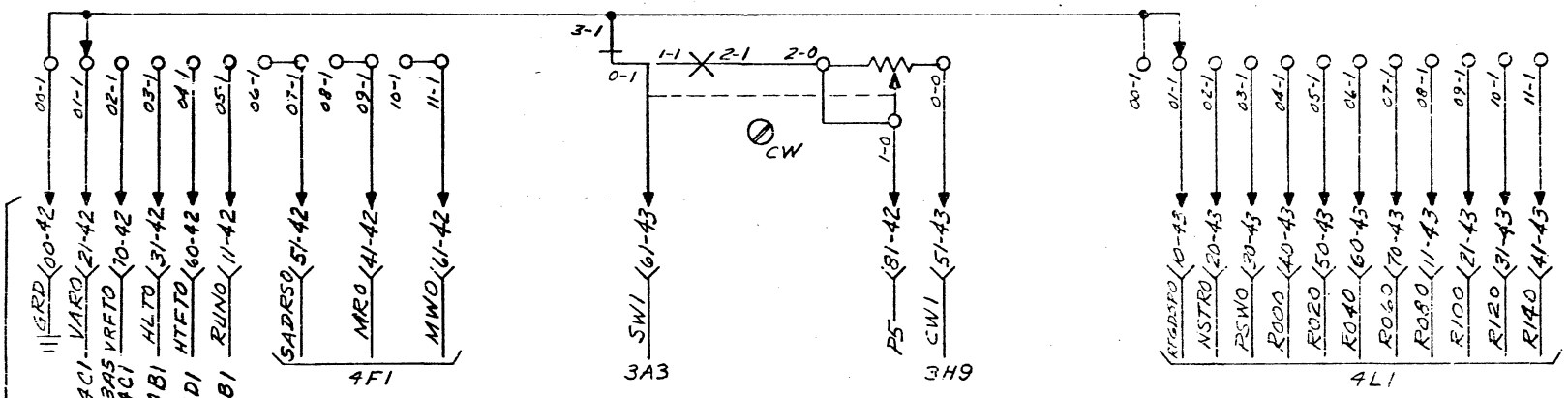
A B C D E F G H J K L M N P R

1 2 3 4 5 6 7 8 9

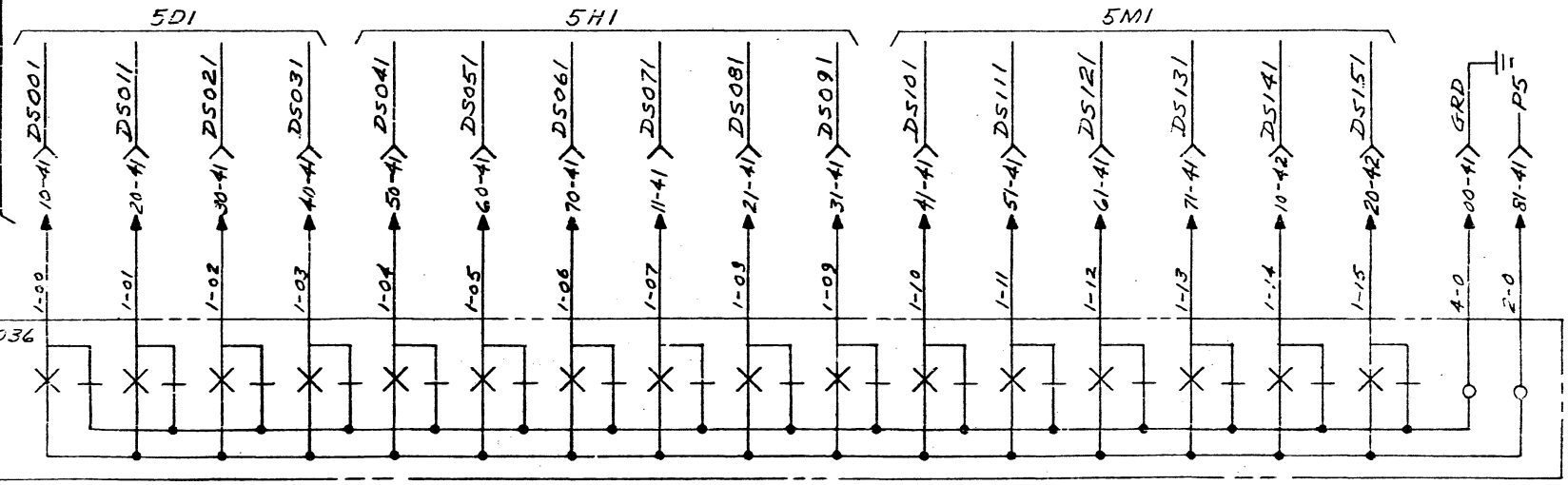
S3 (MODE CONTROL)

S4 (SPEED CONTROL)

S5 (REGISTER DISPLAY)



PART OF DISPLAY CONTROLLER BOARD (DSP)



NOTES: 1. UNLESS OTHERWISE SPECIFIED, APPARATUS IS PART OF CONTROL PANEL.

MADE BY	APPROVAL				
C. Ellsworth JUN.18,'69	E. A. White June 25, 69	DES.		REV.	B
ISSUED JUL 18 1969		CHKR.	DR		

DWG. NO. (FS 31) 70B113003
CONT ON SHEET 7 SH NO. 6

DIST

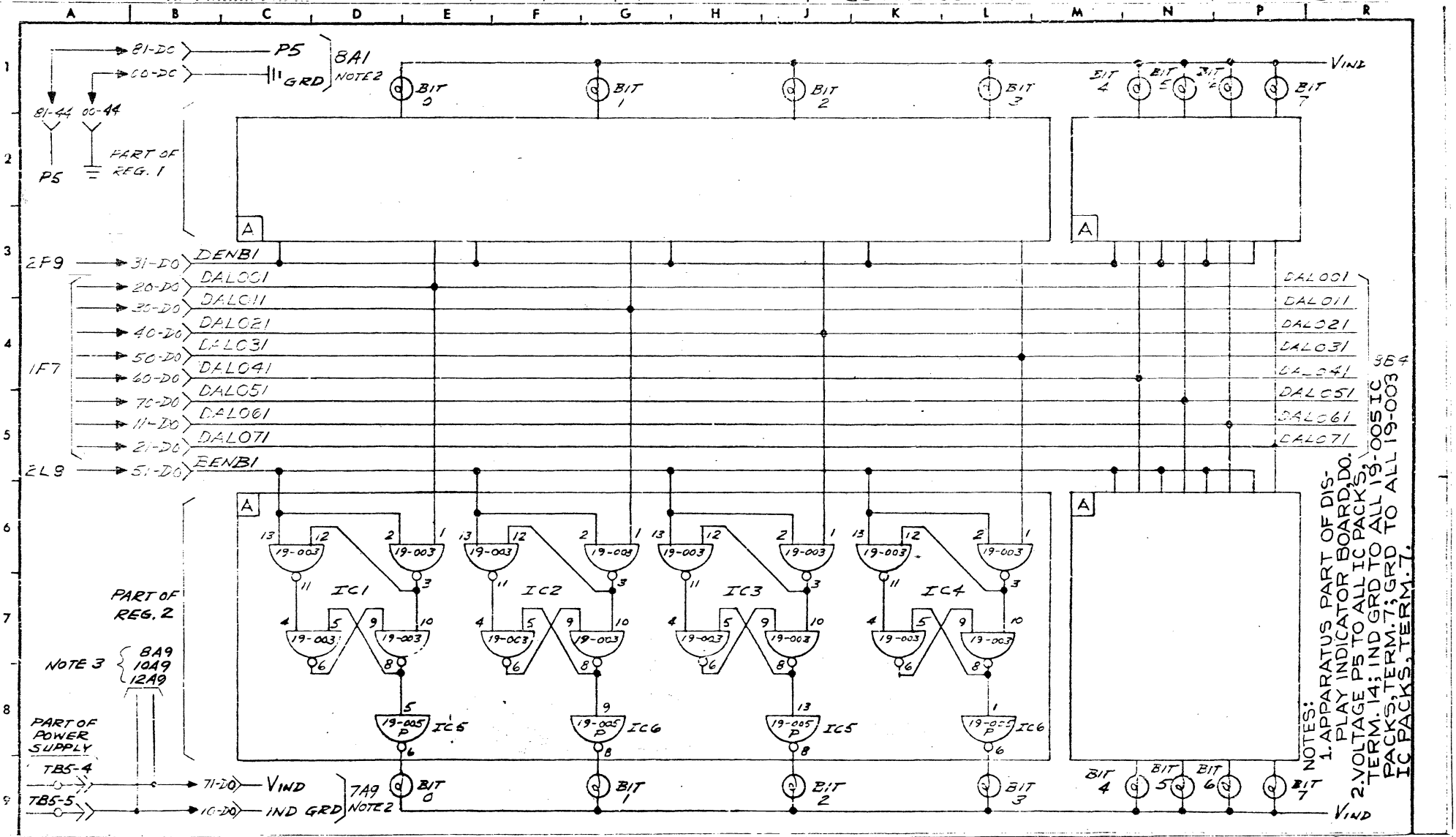
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
DISPLAY CONTROLLER
FMF GE-PAC 30 | FCF

DWG NO (FS31) 70B113003
CONT ON SHEET 8 SH NO 7



MADE BY C. Ellsworth JUN. 18, 69
APPROVAL E. A. White June 25, 69
DES.
CHKR. DK
REV. B

DWG NO (FS31) 70B113003
CONT ON SHEET 8 SH NO 7

JUL 18 1969

DIST.

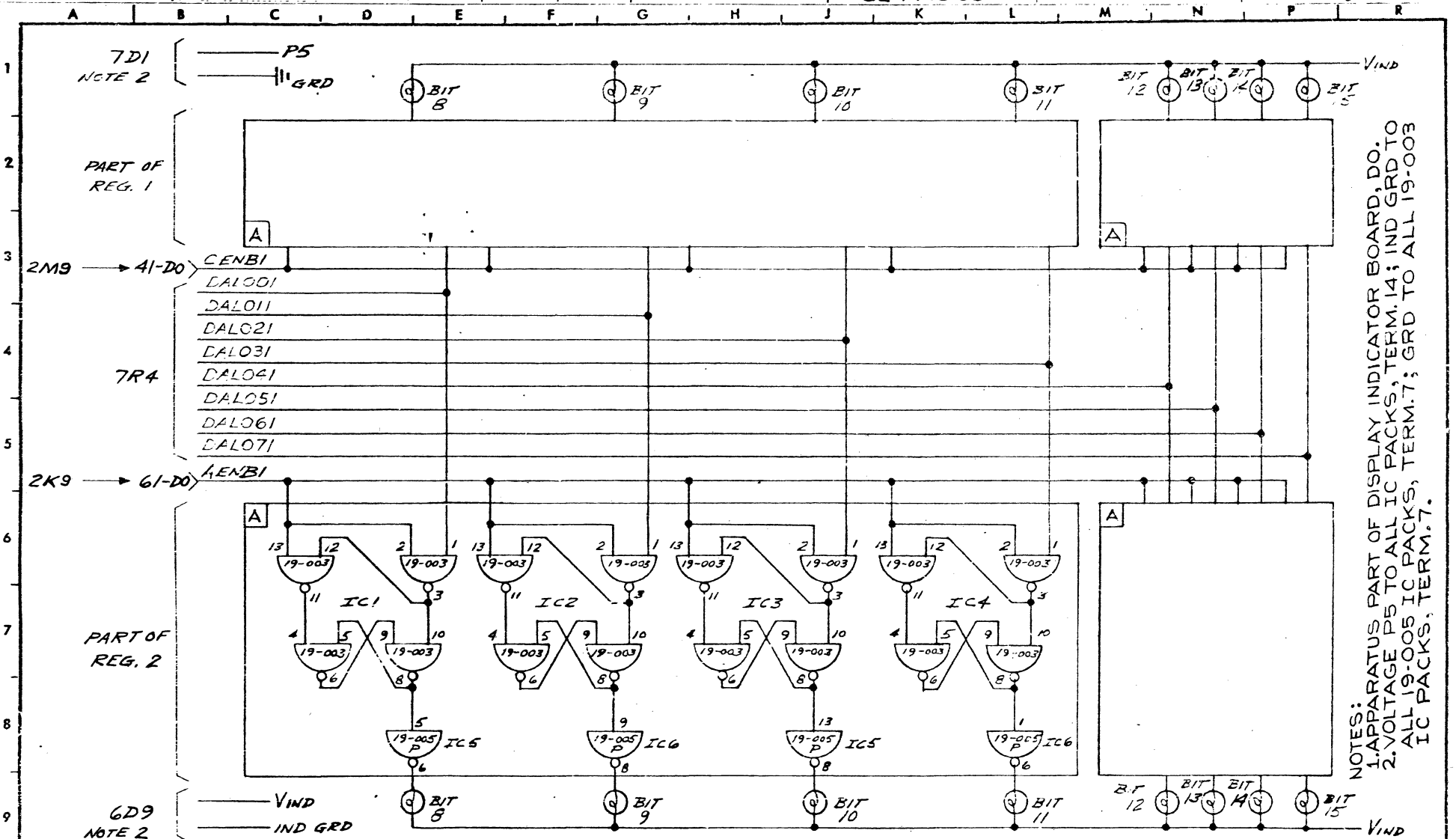
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
DISPLAY CONTROLLER
FMF GE-PAC 30 | FSC

DWG NO (FS31)
70B113003
CONT ON SHEET 9 SH NO 8



NOTES:
1. APPARATUS PART OF DISPLAY INDICATOR BOARD, DO.
2. VOLTAGE P5 TO ALL IC PACKS, TERM. 14; IND GRD TO ALL 19-003 IC PACKS, TERM. 7; GRD TO ALL 19-003 IC PACKS, TERM. 7.

MADE BY	APPROVAL	DES.	REV		DWG NO (FS31)
C. Ellsworth JUN. 18, '69	E.G. White June 25, 69	CHKR. OR	B		70B113003
ISSUED JUL 18 1969					CONT ON SHEET 9 SH NO 8

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
DISPLAY CONTROLLER
FMF GE-PAC 30 FCF

DWG NO (FS31)
70B113003
CONT. ON SHEET F SH NO 9

BACK PANEL MAP

CONN POS	21																				
MOTH. BD	DSP																				
VERT. POS	HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS				
	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2		
22																					
21																					
20																					
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02																					
01																					
00																					

1

22	PS	GND	
21			
20		ENBCO	
19	SNGLO	ESNCO	
18	CATNO	FSNOO	
17	SCLRO	ARSTI	
16		SWATLO	
15	SYNO	ATNO	
14			
13	SRO	CL070	
12	DRO	CL060	
11	DAO	[illegible]KRTO	
10	ADRSO	CMDO	
09	DRL030	DRL070	
06	DRL020	DRL060	
07	DRL010	DRL050	
06	DRL000	DRL040	
05	DAL030	DAL070	
04	DAL020	DAL060	
03	DAL010	DAL050	
02	DAL000	DAL040	
01	PIS	NIS	
00	PS	GND	

0

MADE BY E. Ellsworth JUN. 18, '69
ISSUED JUL 18 1969

APPROVAL E. A. White June

DES.
CHKR. OR

REV. B

DWG. NO. (FS31)
70B113003
CONT ON SHEET F SH NO 9

GENERAL ELECTRIC

PROCESS COMPUTERS
PHOENIX ARIZONA

TITLE FUNCTIONAL SCHEMATIC
READ ONLY MEMORY SWITCH

DRAWING NUMBER 70B113004 | CONT. 0A | PAGE 0
FIRST MADE FOR GE-PAC 30
(FS38)

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
C	ISSUED				

REISSUED

*R Isaacs

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME

REISSUED

(FS38)

MADE BY C. Ellsworth JUN. 18, '69
ISSUED July 18, 1969
APPROVAL DR E. G. White JUNE 26, 69
REV. C

DWG. NO. 70B113004 | CONT. 0A | PAGE 0
PRINTS TO: K7-08

PCE 2981

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
READ ONLY MEMORY SWITCH
FMF GE-PAC 30 | FCF

DWG NO (FS38) 70B113004
CONT. ON SHEET 1 SH NO 0A

SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
SHEET INDEX SUPPORTING INFORMATION	0A	1	2																		
ADDRESS BUFFERS	1	1	1																		
"X" SWITCH SELECT	2	1	1																		
"X" SWITCH SELECT	3	1	1																		
"X" SWITCH SELECT	4	1	1																		
"X" SWITCH SELECT	5	1	1																		
"Y" SWITCH SELECT	6	1	1																		
"Y" SWITCH SELECT	7	1	1																		
"DX" SWITCH SELECT	8	1	1																		
"DX" SWITCH SELECT	9	1	1																		
"DY" SWITCH SELECT	10	1	1																		
RMSTRO CONTROL	11	1	2																		
BACK PANEL MAP	12	1	2																		
BLOCK DIAGRAM	13	1	1																		
ISSUE DATE		2-10-68	4-27-69																		

SUPPORTING INFORMATION

CATEGORY	PART NO.
MOTHER BOARD ROM SWITCH (MOD 2 & MOD 3)	32-068R02
ROM SWITCH (MOD 4)	32-068F01R05

SHEET INDEX NOTES:

1. CHANGES ON THIS DRAWING SHALL REQUIRE ONLY THE REISSUE OF SHEETS AFFECTED.
2. THE ISSUE OF THIS SHEET SHALL DETERMINE THE LATEST ISSUE OF THIS DRAWING.

MADE BY C. Ellsworth JUN. 18, '69
ISSUED JUL 18 1969
APPROVAL E. A. White June 26, 69
DES.
CHKR. DR
REV. C

DWG. NO. (FS38) 70B113004
CONT ON SHEET 1 SH NO. 0A

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --

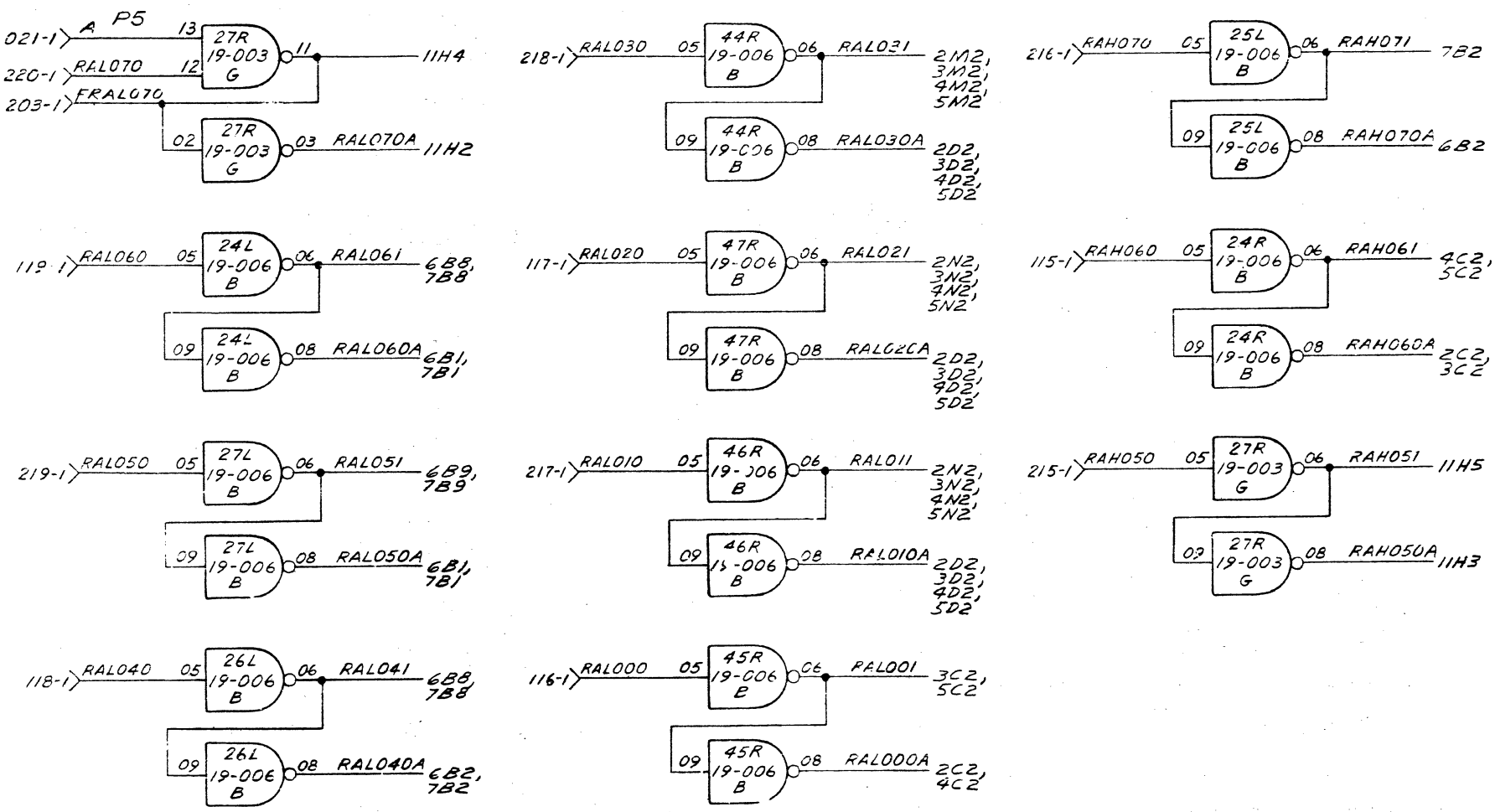
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
READ ONLY MEMORY SWITCH
FMF GE-PAC 30 | FCF

DWG NO (FS38) 70B113004
CONT. ON SHEET 2 SH NO 1

ADDRESS BUFFERS

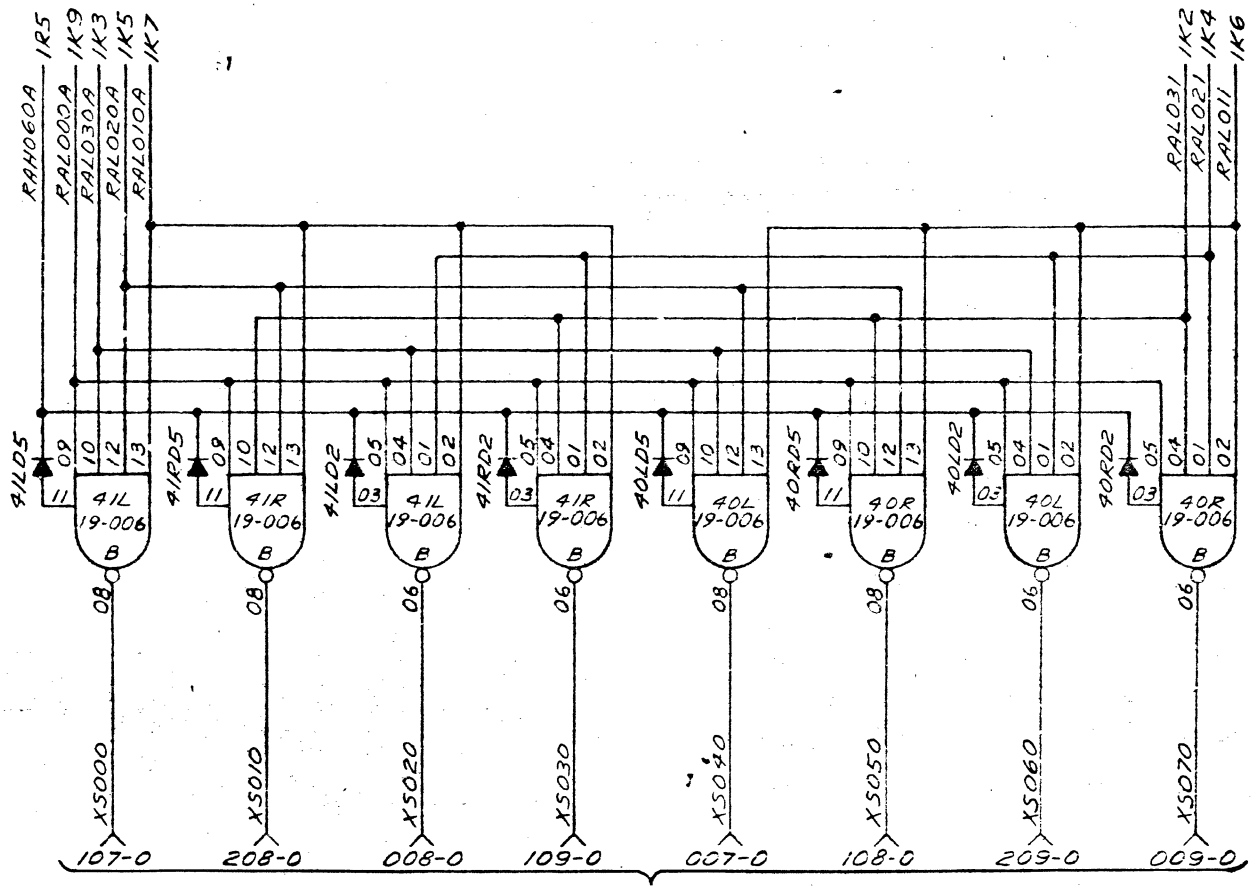


MADE BY	APPROVAL			
E. Ellsworth JUN. 18, '69	E. A. White June 26, 69	DES.		C
ISSUED JUL 18 1969		CHKR.	DR	

DWG. NO. (FS38) 70B113004
CONT ON SHEET 2 SH NO. 1

DIST.	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING - APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES	GENERAL ELECTRIC PROCESS COMPUTER PHOENIX	TITLE FUNCTIONAL SCHEMATIC READ ONLY MEMORY SWITCH FMF GE-PAC 30 FCF	DWG NO (FS38) 70B113004 CONT ON SHEET 3 SH NO 2
		√	±	±	±			

"X" SWITCH SELECT



MADE BY	APPROVAL	DES.	REV.		DWG NO (FS38) 70B113004
E. Ellsworth JUN.18,'69	E.A White June 26	CHKR. DR	C		CONT ON SHEET 3 SH NO. 2
ISSUED JUL 18 1969					

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

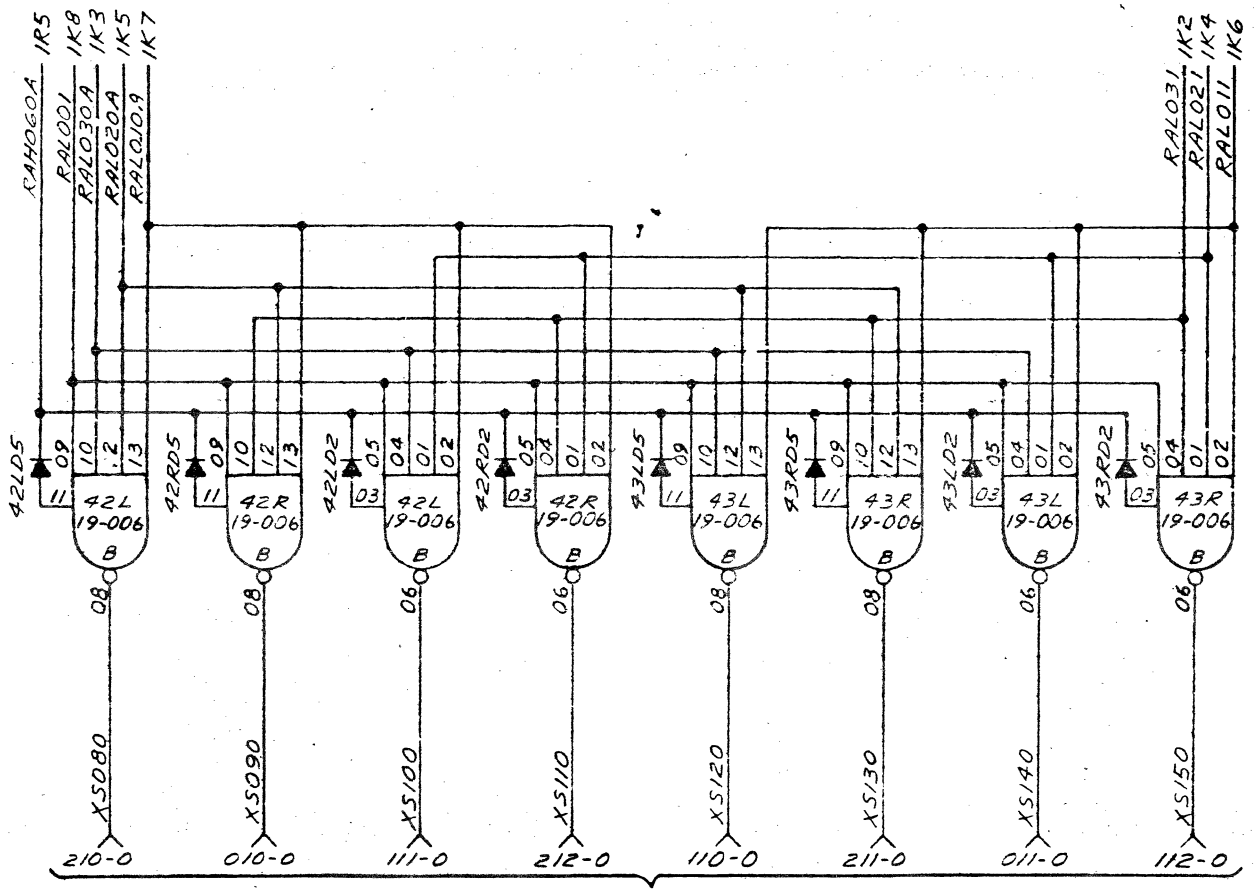
TITLE FUNCTIONAL SCHEMATIC
READ ONLY MEMORY SWITCH
FMF GE-PAC 30 | FCF

DWG NO (FS38) 70B113004
CONT ON SHEET 4 SH NO 3

A B C D E F G H J K L M N P R

1 2 3 4 5 6 7 8 9

"X" SWITCH SELECT



1FS40 OR 1FS39

MADE BY C. Ellsworth JUN. 18,69
ISSUED JUL 18 1969
APPROVAL E.G White June 26, 69
DES.
CHKR. DR
REV C

DWG. NO (FS38) 70B113004
CONT ON SHEET 4 SH NO. 3

DIST

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

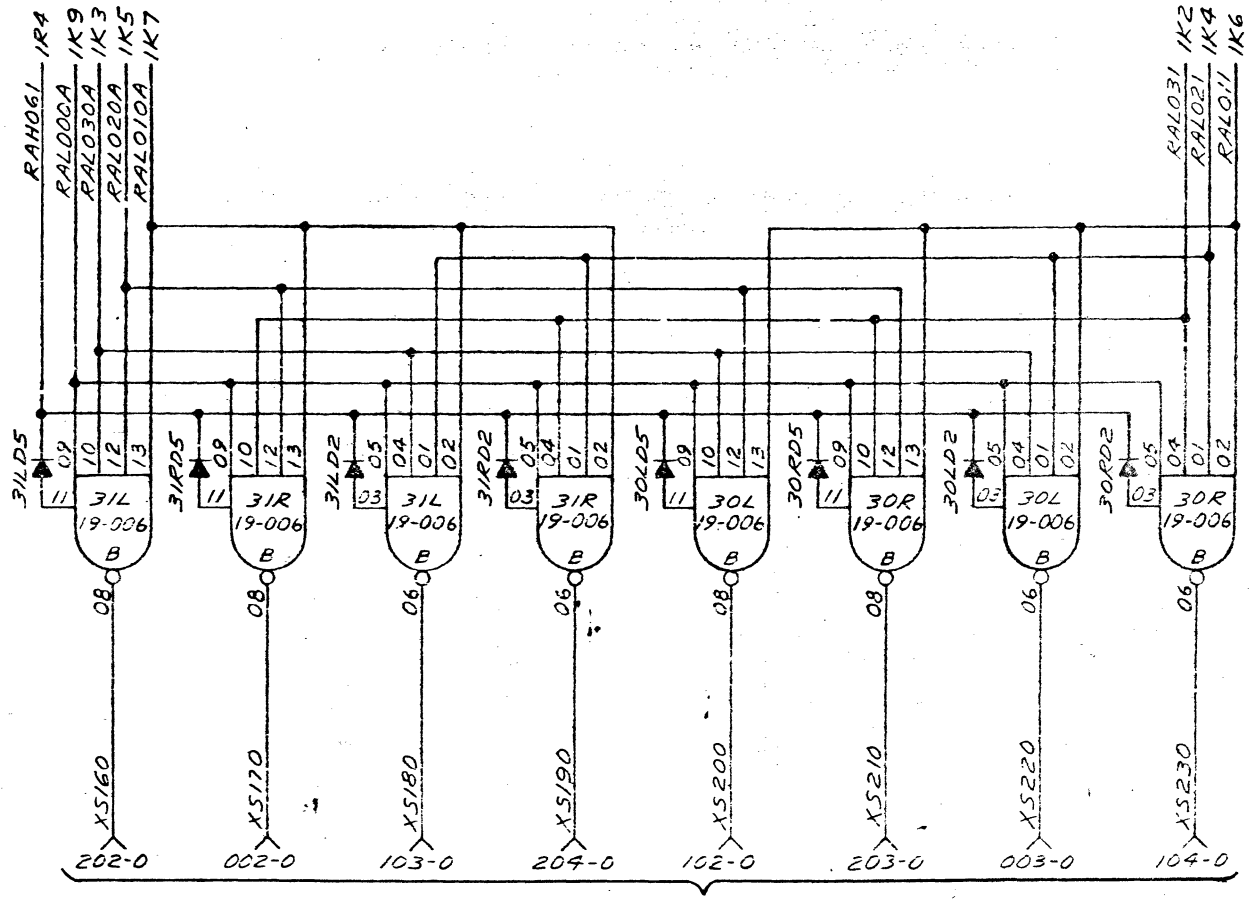
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS		
		FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
READ ONLY MEMORY SWITCH
FMF GE-PAC 30 | FCF

DWG NO (FS38) 70B113004
CONT ON SHEET 5 SH NO 4

"X" SWITCH SELECT



1FS40 OR 1FS39

MADE BY E. Ellsworth JUN. 18; 69
ISSUED JUL 18
APPROVAL E. G. White June 26, 69
DES.
CHKR. DR
REV. C

DWG. NO. (FS38) 70B113004
CONT ON SHEET 5 SH NO. 4

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS		
		FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

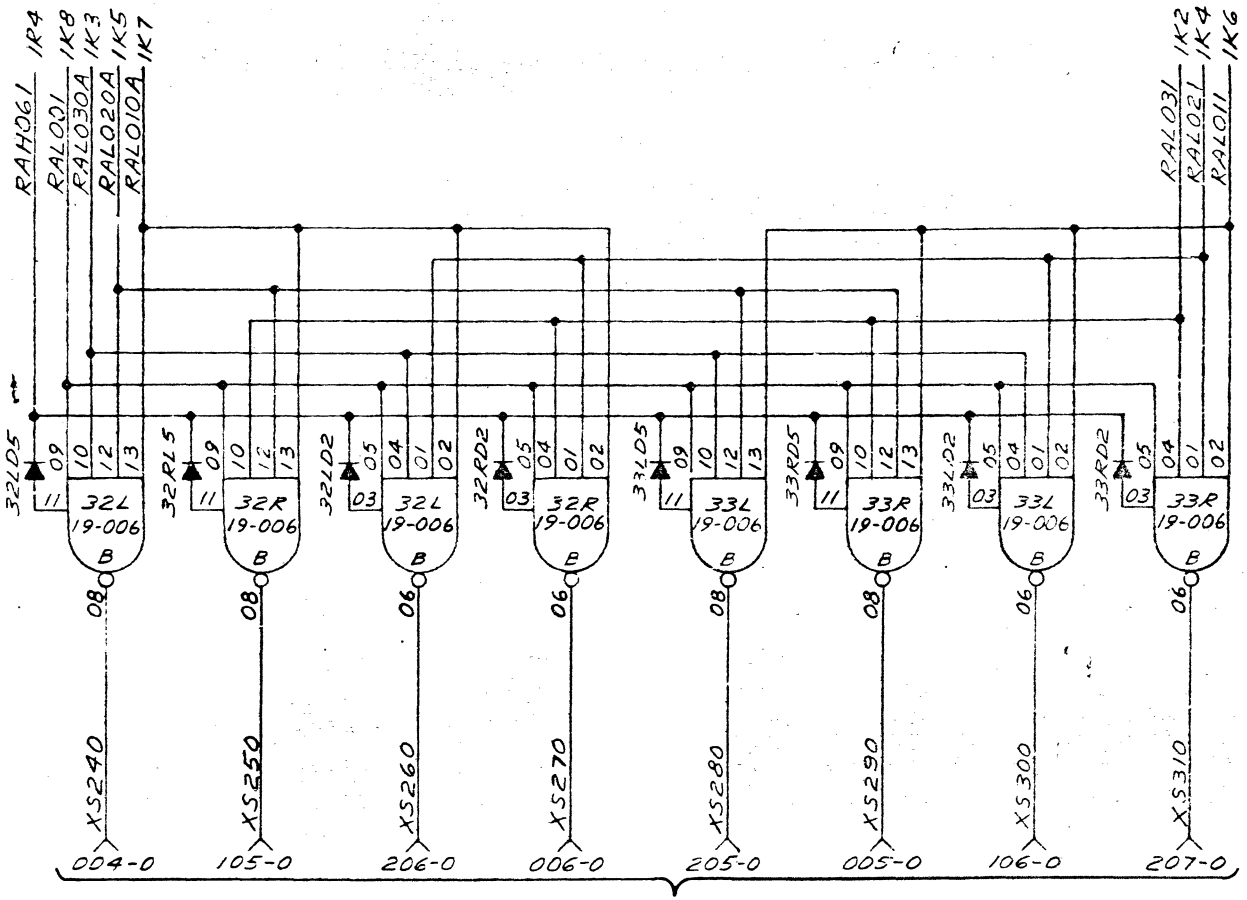
GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
READ ONLY MEMORY SWITCH
FMF GE-PAC 30 | FCF

DWG NO (FS 38) 70B113004
CONT ON SHEET 6 SH NO 5

A B C D E F G H J K L M N P R

"X" SWITCH SELECT



1FS40 OR 1FS39

DATE BY	APPROVAL			
G. Ellsworth JUN.23,69	P. J. White	DES		C
JUL 18 1969	June 26, 69	CHKR	DR	REV.

DWG NO (FS 38) 70B113004
CONT ON SHEET 6 SH NO 5

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
READ ONLY MEMORY SWITCH
FMF GE-PAC-30 | FCF

DWG NO (FS38) 70B113004
CONT. ON SHEET 7 SH NO 6

A B C D E F G H J K L M N P R

"Y" SWITCH SELECT

1E5 RAL060A
1E7 RAL050A
1E9 RAL040A
1R3 RAH070A

22L 19-005 P — 08 70-12
22LD5
22R 19-005 P — 08 11-12
22RD5
22L 19-005 P — 06 61-12
22LD2
22R 19-005 P — 06 20-12
22RD2
23L 19-005 P — 08 70-13
23LD5
23R 19-005 P — 08 11-13
23RD5
23L 19-005 P — 06 61-13
23LD2
23R 19-005 P — 06 20-13
23RD2

35-039 A

P5

50-12 02R02 YS001 017-0
21-12 02R03 YS011 117-0
41-12 02R04 YS021 217-0
30-12 02R01 YS031 016-0

1FS40 OR 1FS39

40-12 51-12 31-12 60-12 P5

35-039 A

50-13 03R01 YS041 115-0
21-13 03R04 YS051 015-0
41-13 03R03 YS061 216-0
30-13 03R02 YS071 116-0

1FS40 OR 1FS39

1E8 RAL041
1E4 RAL061
1E6 RAL051

10R1 CDO
205-1 CDO 01 0<R 19-006 B CE CD1 789

04C01 2.2MF
04D03 04D01 04D02
04R05 04R04 04R03 N15
NBIAS 7R9, 10R8

NOTES:
ALL RESISTORS ARE 1K.

DRAWN BY E. Ellsworth JUN. 23, '69
APPROVAL
ISSUED JUL 18 1969

DES.
CHKR. DR
REV. C

DWG. NO (FS38) 70B113004
CONT ON SHEET 7 SH NO 6

DIST.

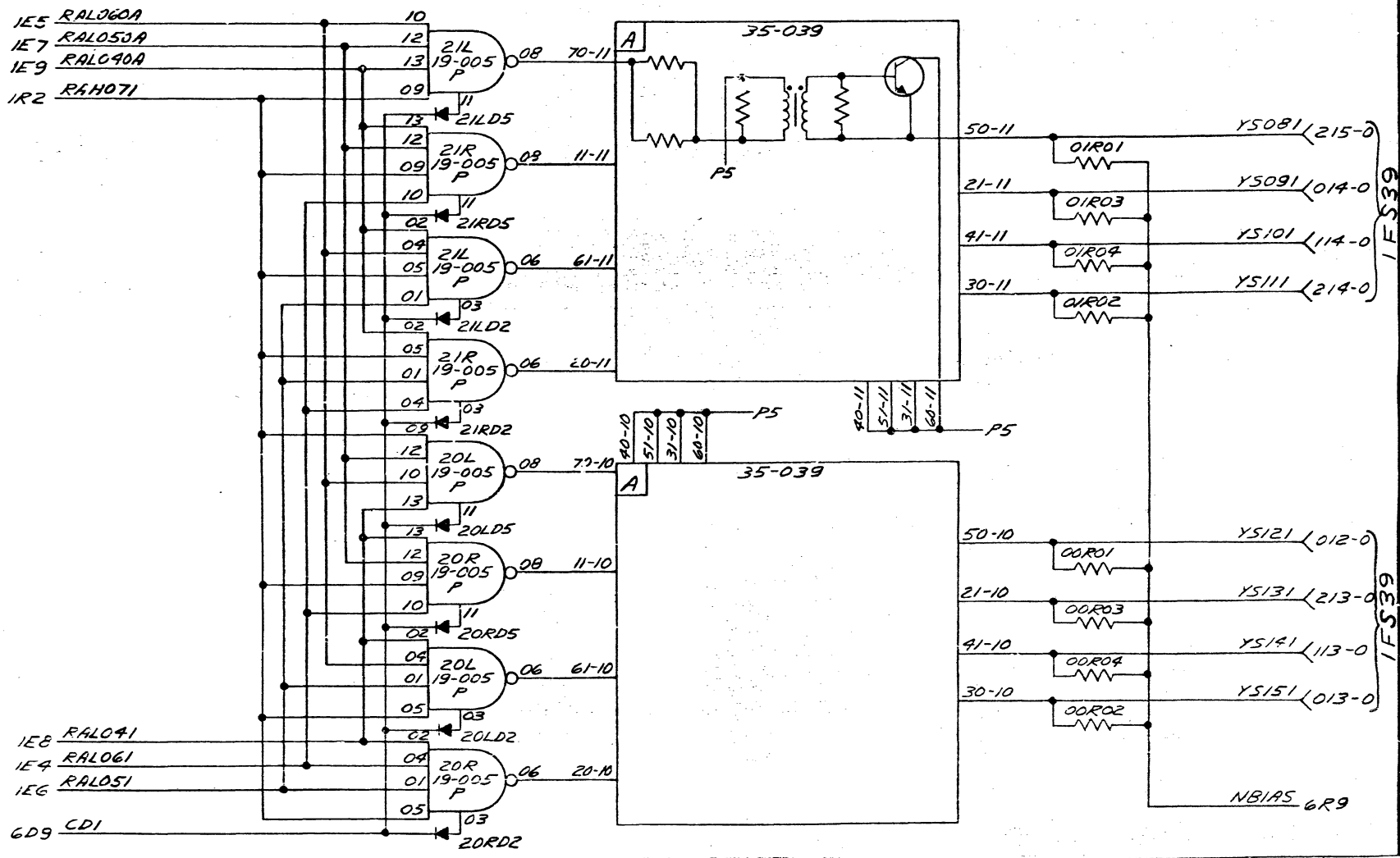
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
READ ONLY MEMORY SWITCH
FMF GE-PAC 30 | FCF

DWG. NO. (FS38) 70B113004
CONT. ON SHEET 8 SH. NO. 7

"Y" SWITCH SELECT



MADE BY	APPROVAL	DES.		REV.	C
E. Ellsworth JUN. 23, '69	E.G. White June 26, 69	CHKR.	DR		
ISSUED JUL 18 1969					

DWG. NO. (FS38) 70B113004
CONT ON SHEET 8 SH. NO. 7

DIST.

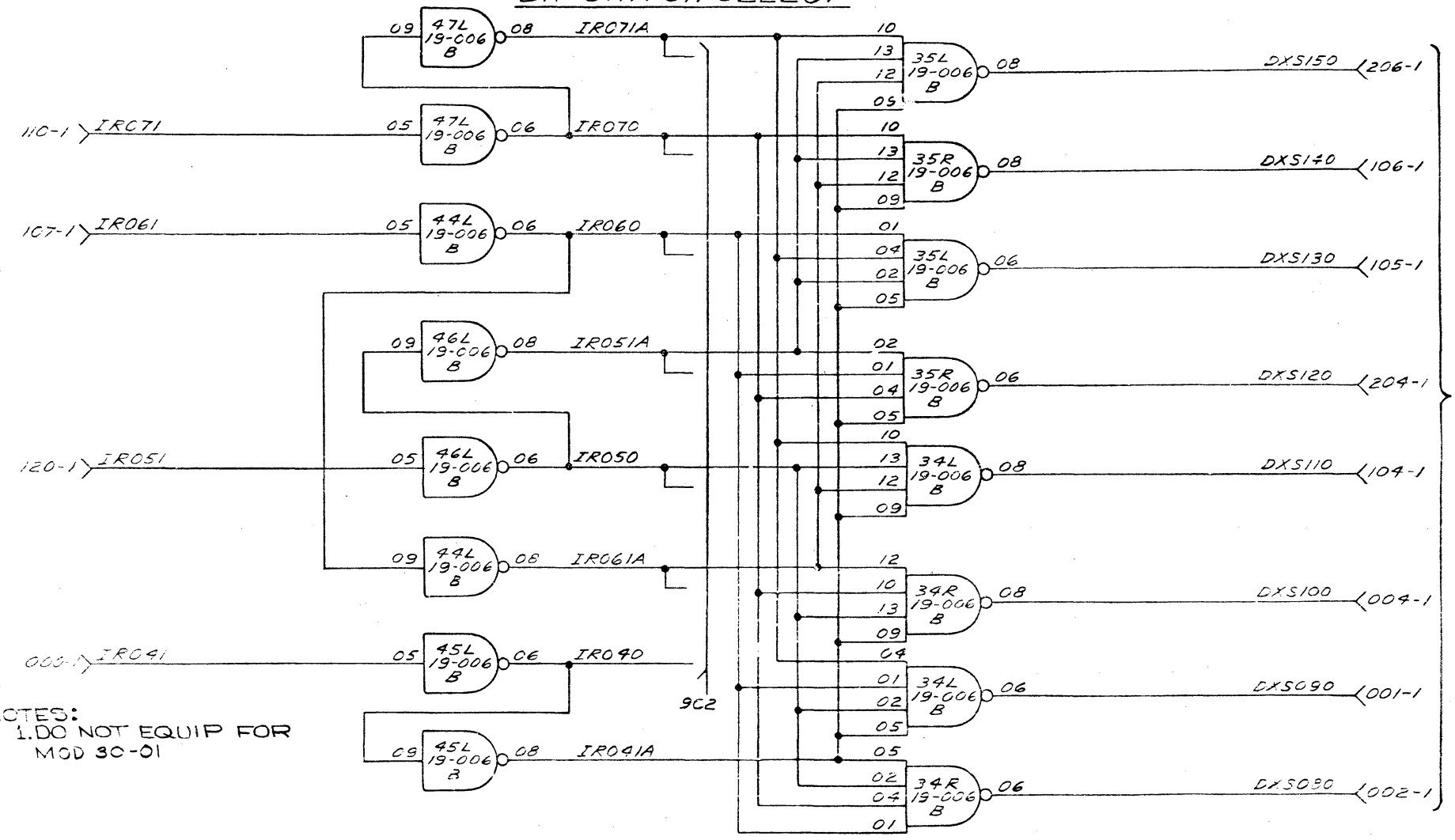
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
READ ONLY MEMORY SWITCH
FMF GE-PAC 30 | FCF

DWG NO (FS 38) 70B113004
CONT. ON SHEET 9 SH NO. 8

"DX" SWITCH SELECT



NOTES:
1. DO NOT EQUIP FOR MOD 30-01

MADE BY E. Ellsworth JUN. 23 '69
APPROVAL E. A. White June 26, 69
DES.
CHKR. UR
REV C

JUL 18 1969

DWG. NO (FS38) 70B113004
CONT. ON SHEET 9 SH NO. 8

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --

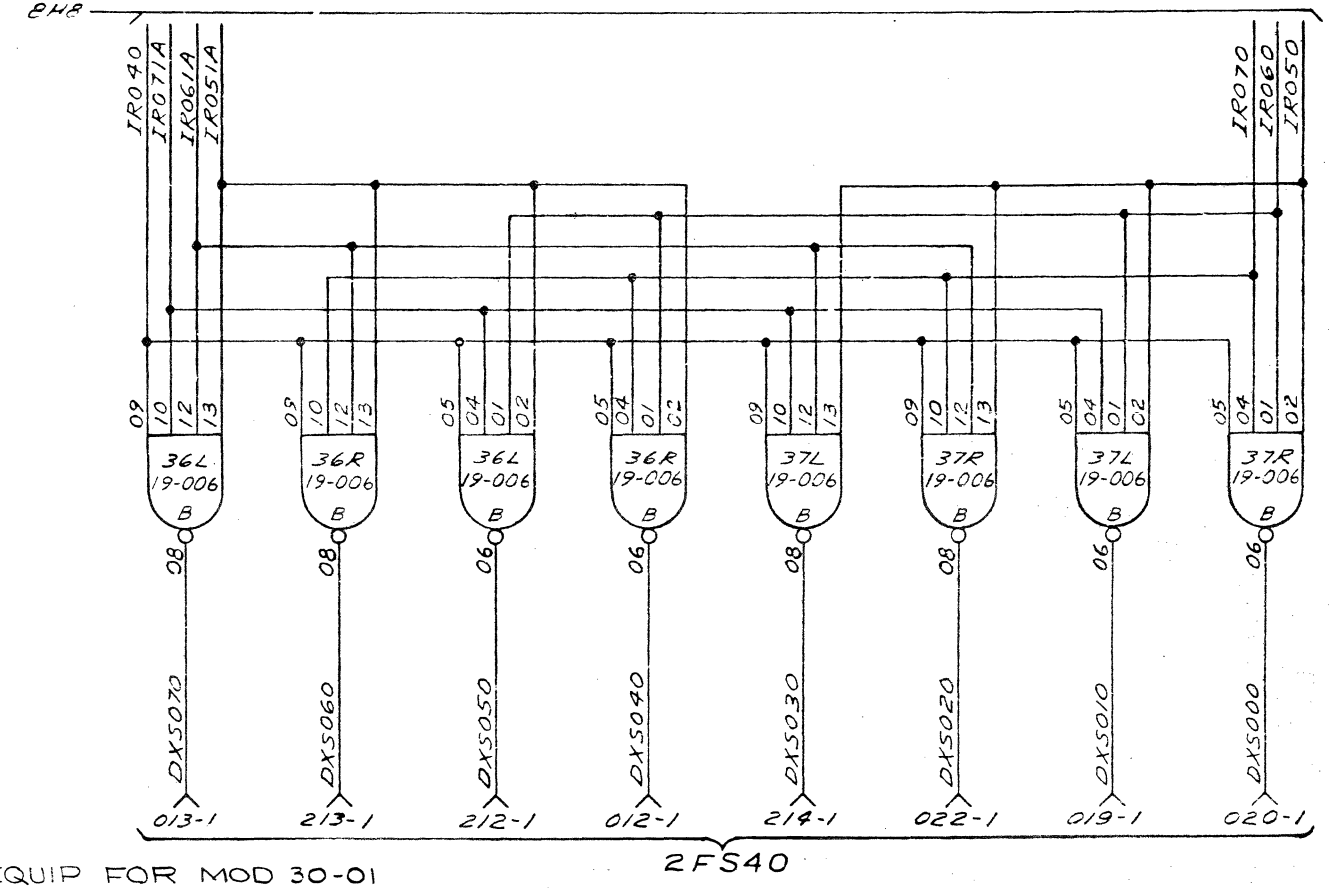
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
READ ONLY MEMORY SWITCH
FMF GE-PAC 30 | FCF

DWG NO (FS 38) 70B113004
CONT ON SHEET 10 SH NO 9

"DX" SWITCH SELECT



NOTES:
1. DC NOT EQUIP FOR MOD 30-01

MADE BY E. Ellsworth JAN. 23, 69
APPROVAL
DES.
CHKR. DR
REV. C

DWG. NO. (FS 38) 70B113004
CONT ON SHEET 10 SH NO. 9

DIST

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:--

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
READ ONLY MEMORY SWITCH
FMF | FCF

DWG NO (FS38)
70B113004
CONT. ON SHEET 11 SH. NO. 10

"DY" SWITCH SELECT

202-1 IR021 IFS45
103-1 IR001 IFS45
109-1 IR011 IFS45
003-1 IR031 IFS45

14R 19-004 G
14L 19-004 G
16L 19-005 P
15L 19-005 P
16R 19-005 P
15R 19-005 P
17R 19-005 P

16LD5
15LD5
16LD2
15LD2
16RD5
15RD5
16RD2
15RD2
17RR2

35-039
A
P5

06R04
06R06
06R05
06R03
04R01
06R01
06R02
04R02

DYS001 011-1
DYS011 015-1
DYS021 019-1
DYS031 010-1
DYS041 108-1
DYS051 208-1
DYS071 009-1
DYS061 102-1
NBIAS 6R9
ENDROMO 018-1
CDO 6A9

2FS40
2FS40

NOTES:
1 DO NOT EQUIP FOR MOD 30-01

MADE BY E. Ellsworth JUN. 23, '69
JUL 18 1969
APPROVAL E. A. White June 26, 69
DES.
CHKR. GR
REV C

DWG. NO. (FS38)
70B113004
CONT ON SHEET 11 SH. NO. 10

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

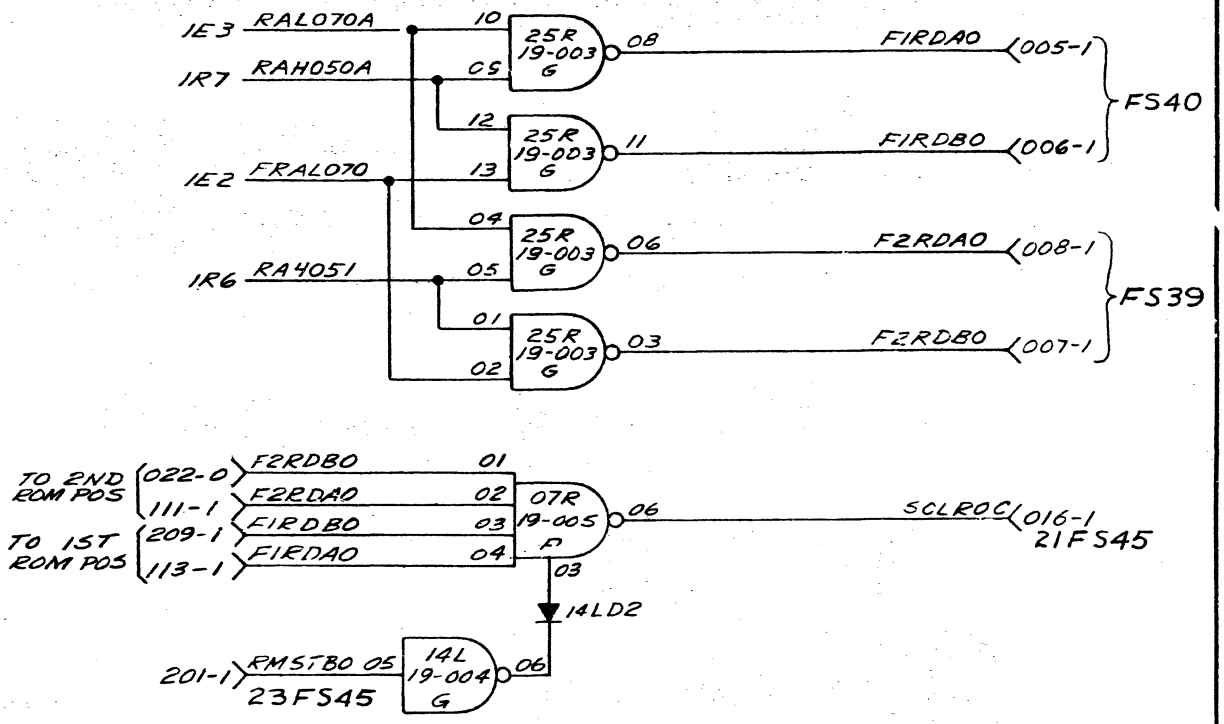
TITLE FUNCTIONAL SCHEMATIC
READ ONLY MEMORY SWITCH
FMF GE-PAC 30 | FCF

DWG NO (FS38) 70B113004
CONT. ON SHEET 12 SH NO 11

A B C D E F G H J K L M N P R

2

RMSTRO CONTROL



MADE BY E. Ellsworth JUN.23,'69
ISSUED JUL 18 1969

APPROVAL E.G. Wuhte June 26, 69

DES.
CHKR. DR

REV. C

LWG. NO (FS38) 70B113004
CONT ON SHEET 12 SH NO. 11

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --
APPLIED PRACTICES | SURFACES: V | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
READ ONLY MEMORY SWITCH
FMF GE-PAC 30 | FCF

DWG NO (FS38) 70B113004
CONT. ON SHEET 13 SH NO 12

BACK PANEL MAP

CONN POS		07																		
MOTH. PD		ROM SWITCH			HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS		
VERT. POS		HORIZ POS																		
		0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2
	22	DXS020	P5	GND																
	21	A	P15	N15																
	20	DXS000	IR051	RAL070																
	19	DXS010	RAL060	RAL050																
	18	ENDROM0	RAL040	RAL030																
	17		RAL020	RAL010																
	16	SCLROC	RAL000	RAH070																
	15	DYS011	RAH060	RAH050																
3	14	DYS021		DXS030																
	13	DXS070	F1RDA0	DXS060																
	12	DXS040		DXS050																
/	11	DYS001	F2RDA0																	
	10	DYS031	IR071																	
	09	DYS071	IR011	F1RDB0																
4	08	F2RDA0	DYS041	DYS051																
	07	F2RDB0	IR061																	
	06	F1RLB0	DXS140	DXS150																
	05	F1RDA0	DXS130	CDO																
	04	DXS100	DXS110	DXS120																
	03	IR031	IR001	FRAL070																
5	02	DXS080	DYS061	IR021																
	01	DXS090		RMSTB0																
	00	IR041	P5	GND																
	22	F2RDB0	P5	GND																
	21			N15																
	20																			
6	19																			
	18																			
	17	YS001	YS011	YS021																
	16	YS031	YS071	YS061																
	15	YS051	YS041	YS081																
7	14	YS091	YS101	YS111																
	13	YS151	YS141	YS131																
	12	YS121	XS150	XS110																
0	11	XS140	XS100	XS130																
	10	XS090	XS120	XS060																
	09	XS070	XS030	XS060																
	08	XS020	XS050	XS010																
8	07	XS040	XS000	XS310																
	06	XS270	XS300	XS260																
	05	XS290	XS250	XS280																
	04	XS240	XS230	XS190																
	03	XS220	XS180	XS210																
	02	YS170	XS200	XS160																
9	01		P15	N15																
	00		P5	GND																

MADE BY C. Ellsworth JUN. 23, '69
ISSUED JUL 18 1969
APPROVAL
DES.
CHKR. DR
REV. C

DWG. NO (FS-38) 70B113004
CONT ON SHEET 13 SH NO 12

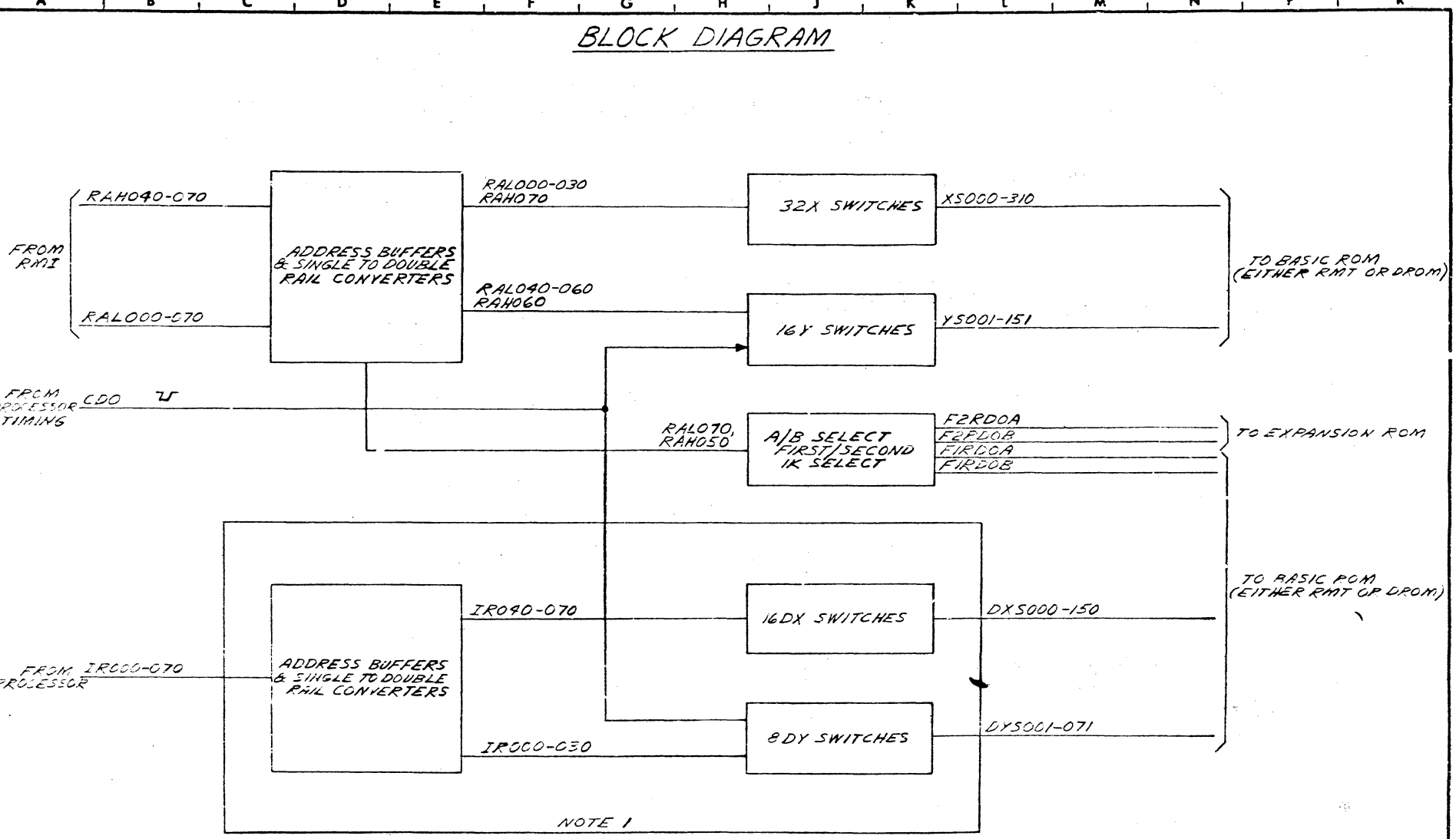
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS		
		FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

FUNCTIONAL SCHEMATIC
READ ONLY MEMORY SWITCH
FMF GE-PAC 30 | FCF

DWG. NO (FS38) 70B113004
CONT. ON SHEET F SH NO 13

BLOCK DIAGRAM



LADLEY	APPROVAL									
C. Elmore JUN. 23, 69		DES.		REV.	C					
ISSUED JUL 18 1969		CHKR.								

DWG. NO (FS38) 70B113004
CONT ON SHEET F SH NO. 13

GENERAL ELECTRIC

PROCESS COMPUTERS
PHOENIX ARIZONA

TITLE FUNCTIONAL SCHEMATIC
ROM TRANSFORMER

DRAWING NUMBER 70B113005 | CONT. 0A | PAGE 0

FIRST MADE FOR GE-PAC 30
(FS39)

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
C	ISSUED				

REISSUED

C issued

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME

REISSUED

MADE BY	APPROVAL	REV.	DWG. NO.	CONT.	PAGE
E. Ellsworth JUN. 23 69	E. A. White Jun 26, 69		70B113005	0A	0
ISSUED July 18, 1969			PRINTS TO: K7-08		

PCE 29M

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING				
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
ROM TRANSFORMER
FMF GE-PAC 30 | FCF

DWG NO (FS39)
70B113005
CONT ON SHEET 1 SH NO 0A

SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
SHEET INDEX SUPPORTING INFORMATION	0A	1	2																		
MATRIX	1	1	1																		
READOUT AMP	2	1	2																		
STROBE LOGIC	3	1	2																		
BACK PANEL MAP	4	1	1																		
BLOCK DIAGRAM	5	1	1																		
	ISSUE DATE	1-10-68	1-27-69																		

SUPPORTING INFORMATION

CATEGORY	PART NO
MOTHER BOARD ROM TRANSFORMER (RMT)	32-017R03 52-017F01R05 32-017F02R05 52-017F03R05 52-017F04R05 52-017F05F02

SHEET INDEX NOTES:

1. CHANGES ON THIS DRAWING SHALL REQUIRE ONLY THE REISSUE OF SHEETS AFFECTED.
2. THE ISSUE OF THIS SHEET SHALL DETERMINE THE LATEST ISSUE OF THIS DRAWING.

MADE BY E. Ellsworth JUN. 23. 69
ISSUED JUL 18 1969

APPROVAL E. A. White June 26, 69

DES.
CHKR DR

REV. C

DWG NO (FS39)
70B113005
CONT ON SHEET 1 SH NO 0A

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS		
		FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
ROM TRANSFORMER
FMF GE-PAC 30 | FCF

DWG NO (FS39)
70B113005
CONT. ON SHEET 2 SH NO 1

A B C D E F G H J K L M N P R

1 2 3 4 5 6 7 8 9

MATRIX

6FS38

213-0 YS151
113-0 YS141
013-0 YS131
212-0 YS121
014-0 YS111
114-0 YS101
214-0 YS091
015-0 YS081
115-0 YS071
215-0 YS061
016-0 YS051
116-0 YS041
216-0 YS031
017-0 YS021
117-0 YS011
217-0 YS001

16 x 32 DIODE MATRIX

WORD LINE

Y

X X

TYPICAL

XS000 XS010 XS020 XS030 XS040 XS050 XS060 XS070
107-0 008-0 208-0 109-0 207-0 108-0 009-0 209-0
2FS38

XS080 XS090 XS100 XS110 XS120 XS130 XS140 XS150
010-0 210-0 111-0 211-0 112-0 011-0 211-0 112-0
3FS38

XS160 XS170 XS180 XS190 XS200 XS210 XS220 XS230
002-0 202-0 103-0 003-0 102-0 003-0 203-0 104-0
4FS38

XS240 XS250 XS260 XS270 XS280 XS290 XS300 XS310
204-0 115-0 006-0 206-0 005-0 215-0 106-0 207-0
5FS38

MADE BY E. Ellsworth JUN 23,'69
CHKD JUL 18 1969
APPROVAL E. A. White June 26, 69
DES.
CHKR DR
REV C

DWG NO (FS39)
70B113005
CONT ON SHEET 2 SH NO 1

DIST.

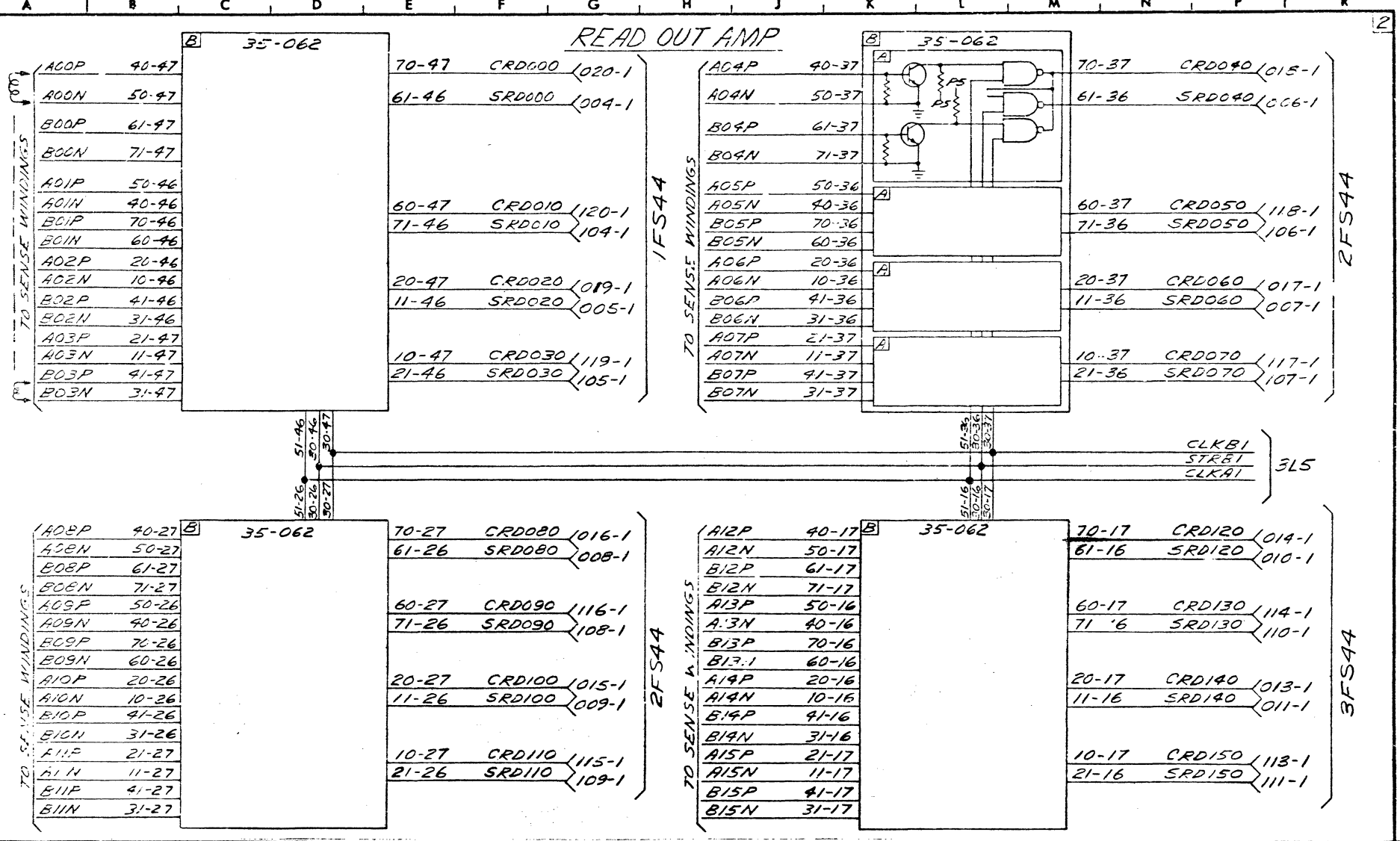
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS		
		FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
ROM TRANSFORMER
FMF GE-PAC 30 | FCF

DWG NO (FS39)
70B113005
CONT. ON SHEET 3 SH NO 2



MADE BY S. Ellsworth JUN. 23, 69
ISSUED JUL 18 1969
APPROVAL E. A White June 26, 69
DES.
CHKR. DR
REV. C

DWG NO (FS39)
70B113005
CONT ON SHEET 3 SH NO. 2

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

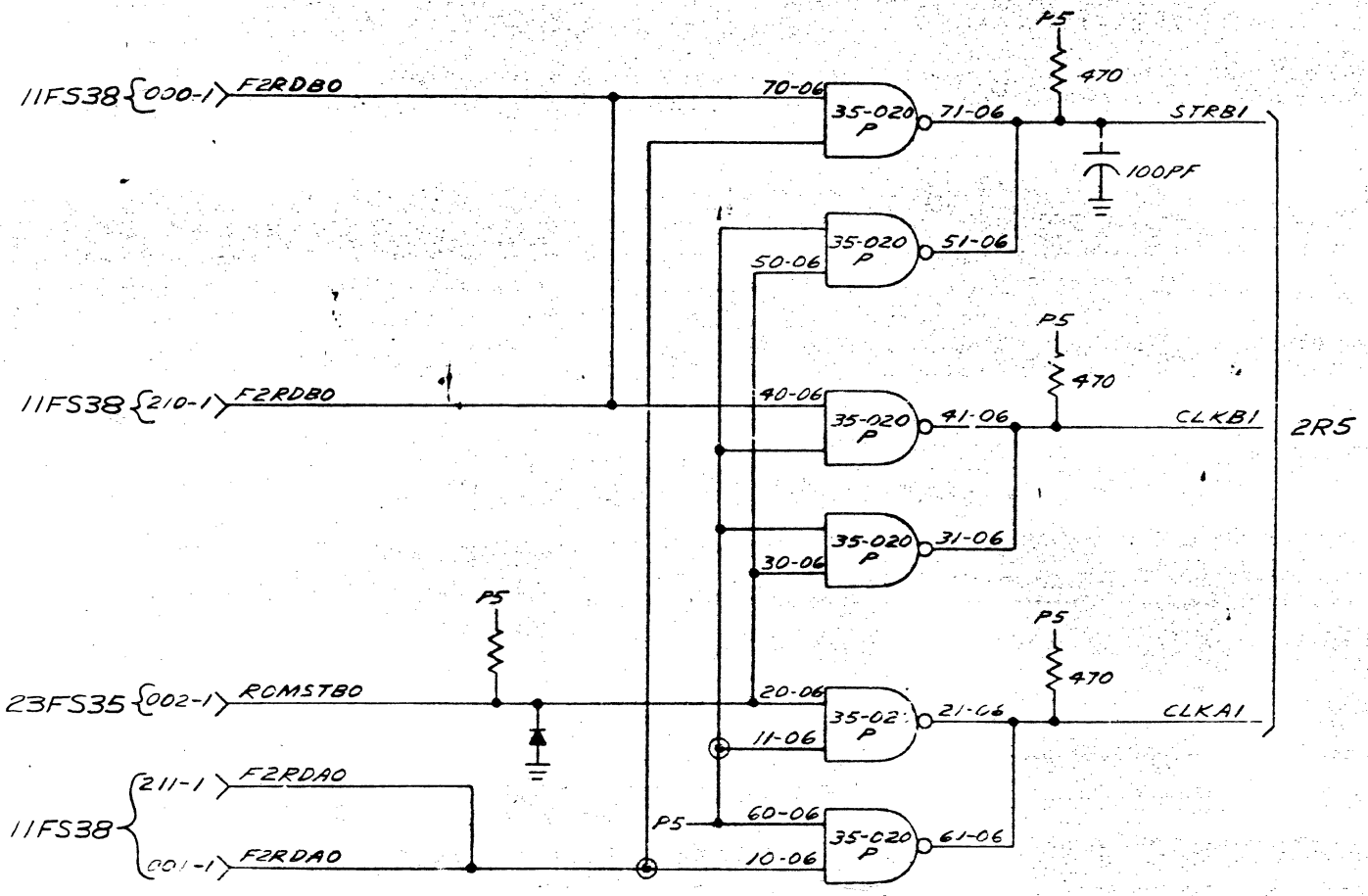
GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
ROM TRANSFORMER
FOR GE-PAC 30 | FCF

DWG NO (FS39)
70B113005
CONT. ON SHEET 4 SH. NO 3

2

STROBE LOGIC



MADE BY C.Ellsworth JUN.23,'69
ISSUED JUL 18 1969

APPROVAL E.A. White June 26, 69

DES.
CHKR DR

C

DWG. NO. (FS39)
70B113005
CONT ON SHEET 4 SH NO. 3

DIST.	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:					GENERAL ELECTRIC PROCESS COMPUTER PHOENIX	TITLE FUNCTIONAL SCHEMATIC ROM TRANSFORMER FOR GE-PAC 30 FCF	DWG NO (FS39) 70B113005
	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES			CONT. ON SHEET 5 SH NO 4
		√	±	±	±			

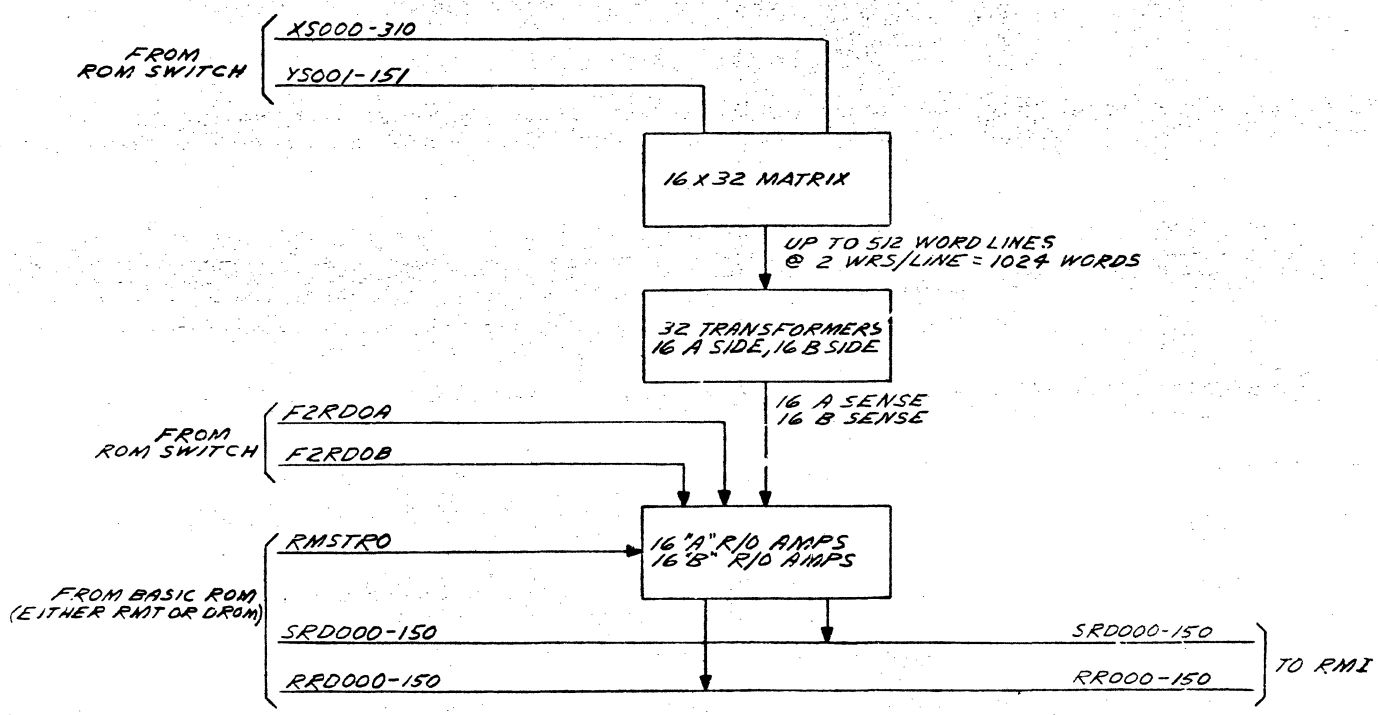
BACK PANEL MAP

CONN. 05	08																			
MOTH. BD	RMT																			
VERT. POS	HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS			
	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2		
22		P5	GND																	
21																				
20	CRD002	CRD010																		
19	CRD020	CRD030																		
18	CRD040	CRD050																		
17	CRD060	CRD070																		
16	CRD080	CRD090																		
15	CRD100	CRD110																		
14	CRD120	CRD130																		
13	CRD140	CRD150																		
12																				
11	SRD140	SRD150	F2RDA0																	
10	SRD120	SRD130	F2RDB0																	
09	SRD100	SRD110																		
08	SRD080	SRD090																		
07	SRD060	SRD070																		
06	SRD040	SRD050																		
05	SRD020	SRD030																		
04	SRD000	SRD010																		
03																				
02	ROMSTB0																			
01	F2RDA0																			
00	F2RDB0	P5	GND																	
22		P5	GND																	
21																				
20																				
19																				
18																				
17	YS021	YS011	YS001																	
16	YS061	YS071	YS031																	
15	YS081	YS041	YS051																	
14	YS111	YS101	YS091																	
13	YS131	YS141	YS151																	
12	XS110	XS150	XS121																	
11	XS130	XS100	XS140																	
10	XS080	XS120	XS090																	
09	XS060	XS030	XS070																	
08	XS010	XS050	XS020																	
07	XS310	XS000	XS040																	
06	XS260	XS300	XS270																	
05	XS280	XS250	XS290																	
04	XS190	XS230	XS240																	
03	XS210	XS180	XS220																	
02	XS160	XS200	XS170																	
01																				
00		P5	GND																	

MADE BY	APPROVAL				DWG. NO (FS39) 70B113005
G. Ellsworth JUN. 23, '69	E. A. White June 26, 69	DES.		REV C	CONT ON SHEET 5 SH NO. 4
ISSUED JUL 18 1969		CHKR.	DR		

DIST.	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—					GENERAL ELECTRIC	TITLE	DWG. NO.
	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES	PROCESS COMPUTER PHOENIX	FUNCTIONAL SCHEMATIC ROM TRANSFORMER FOR GE-PAC 30 1 FCF	(FS39) 70B113005 CONT. ON SHEET F SH. NO. 5
		√	±	±	±			

BLOCK DIAGRAM



MADE BY	APPROVAL	DES.		REV.		DWG. NO. (FS39) 70B113005
E. Ellsworth JUN. 23, 69		CHKR	OR	C		CONT. ON SHEET F SH. NO. 5
ISSUED JUL 1 8 1969						

GENERAL ELECTRIC

PROCESS COMPUTERS
PHOENIX ARIZONA

TITLE FUNCTIONAL SCHEMATIC
DROM TRANSFORMER

DRAWING NUMBER	CONT.	PAGE
70B113006	0A	0

FIRST MADE FOR
GE-PAC 30
(FS40)

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
C	ISSUED				

REISSUED

C reissued

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME

REISSUED

(FS40)

MADE BY	APPROVAL	REV.	DWG. NO.	CONT.	PAGE
C. Ellsworth JUN 23 69	E.C White Jun 26, 69		70B113006	0A	0
ISSUED July 18 1969			PRINTS TO: K7-08		

PCE 28M

DIST.	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING					GENERAL ELECTRIC	TITLE	DWG NO (FS40)
	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENS ONS			PROCESS COMPUTER PHOENIX	FUNCTIONAL SCHEMATIC DROM TRANSFORMER	70B113006
			FRACTIONS	DECIMALS	ANGLES		FMF GE-PAC 30 FCF	CONT ON SHEET 1 SH NO 0A
		√	±	±	±			

SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
SHEET INDEX SUPPORTING INFORMATION	0A	1	2																		
MATRIX	1	1	1																		
MATRIX	2	1	1																		
READ OUT AMP	3	1	1																		
READ OUT AMP	4	1	2																		
STROBE LOGIC	5	1	2																		
BACK PANEL MAP	6	1	1																		
BLOCK DIAGRAM	7	1	1																		
ISSUE DATE		7-10-68	3-27-69																		

SUPPORTING INFORMATION

CATEGORY	PART NO.
MOTHER BOARD DROM TRANSFORMER	32-062

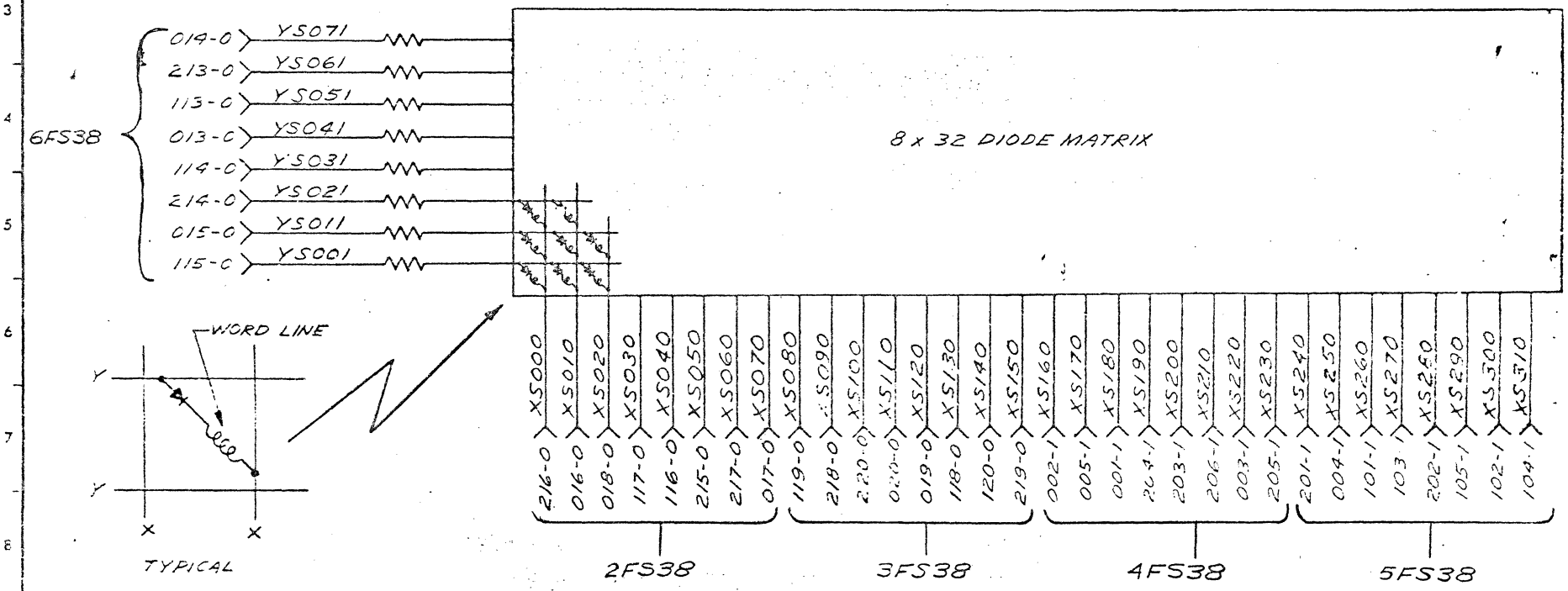
SHEET INDEX NOTES:

1. CHANGES ON THIS DRAWING SHALL REQUIRE ONLY THE REISSUE OF SHEETS AFFECTED.
2. THE ISSUE OF THIS SHEET SHALL DETERMINE THE LATEST ISSUE OF THIS DRAWING.

MADE BY	APPROVAL									DWG NO (FS40)
C. Ellsworth JUN. 23, '69	E. A. White June 26, 69	DES.		REV.	C					70B113006
ISSUED JUL 18 1969		CHKR.	DR							CONT ON SHEET 1 SH NO. 0A

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING					GENERAL ELECTRIC	TITLE FUNCTIONAL SCHEMATIC	DWG NO (FS40)
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENS ONS			PROCESS COMPUTER PHOENIX	DROM TRANSFORMER	70B113006
	√	FRACTIONS ±	DECIMALS ±	ANGLES ±	FMF GE-PAC 30 | FCF	CONT ON SHEET 2	SH NO 1

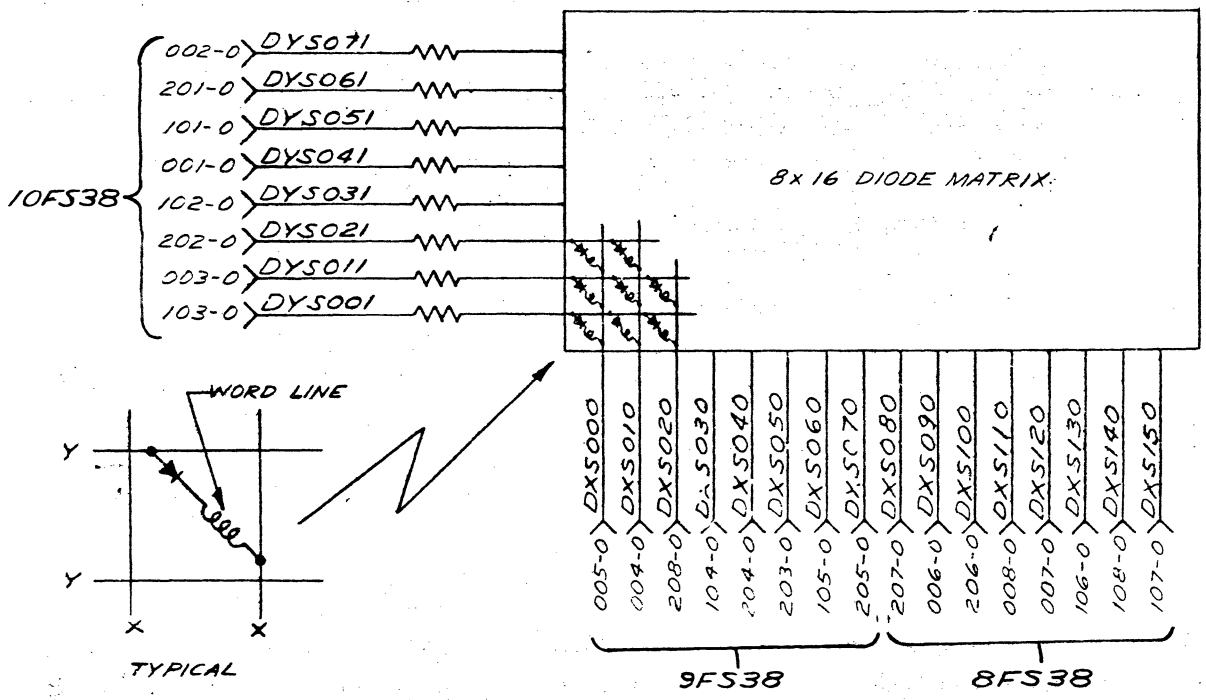
MATRIX



MADE BY	APPROVAL					DWG. NO (FS40)
E. Ellsworth JUN. 23, '69	E.G. White June 26, 69	DES.		REV.	C	70B113006
ISSUED JUL 18 '69		CHKR.	GR			CONT ON SHEET 2 SH NO 1

DIST.	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING					GENERAL ELECTRIC	TITLE	DWG NO
	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES	PROCESS COMPUTER PHOENIX	FUNCTIONAL SCHEMATIC DROM TRANSFORMER	(FS40) 70B113006
		√	±	±	±	FMF GE-PAC 30 1 FCF		CONT ON SHEET 3 SH NO 2

MATRIX



MADE BY	APPROVAL	DES.	REV.		DWG NO
E. Ellsworth JUN. 24, '69	E. A. White June 26, 69	CHKR	C		(FS40) 70B113006
ISSUED JUL 18 1969					CONT ON SHEET 3 SH NO. 2

DIST.

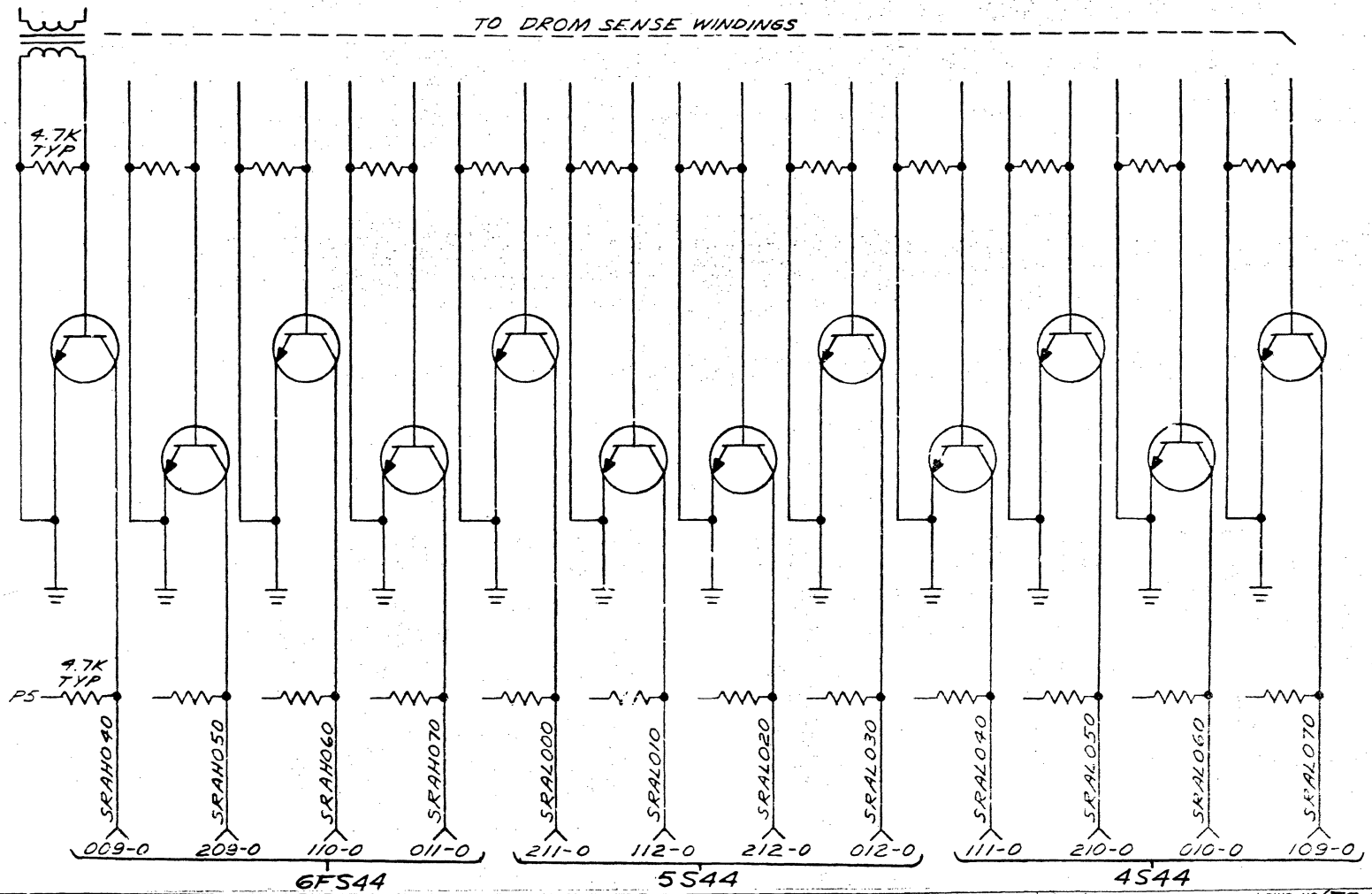
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGULAR ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
DROM TRANSFORMER
FOR GE-PAC 30 | PCF

DWG. NO (FS40)
70B113006
CONT. ON SHEET 4 SH. NO. 3

READ OUT AMP



MADE BY E. Ellsworth JUN. 24, '69
ISSUED JUL 18 1969

APPROVAL E. A. White June 26, 69

DES.
CHKR. DR

REV. C

DWG. NO (FS40)
70B113006
CONT ON SHEET 4 SH NO 3

DIST.

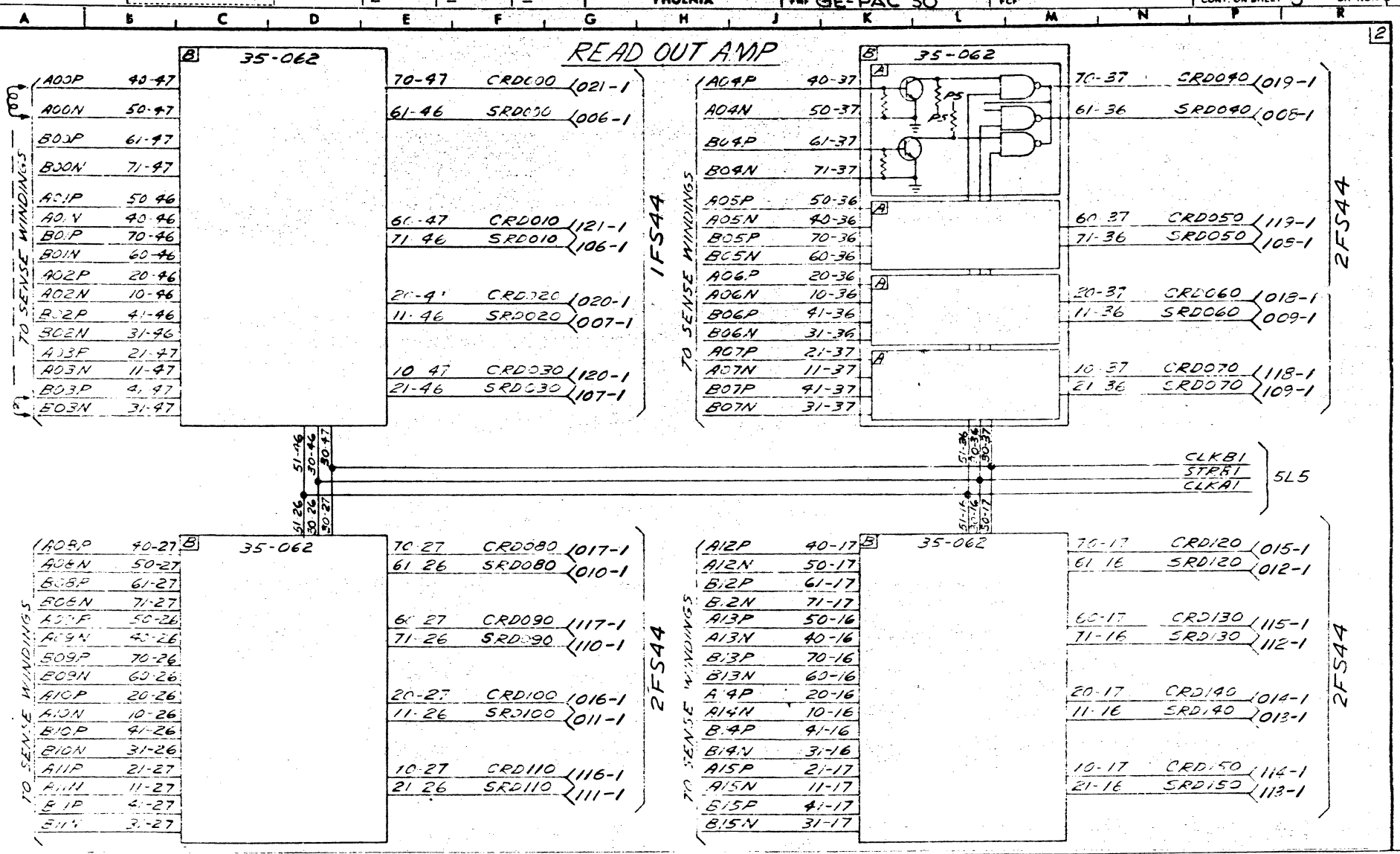
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:--

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
DROM TRANSFORMER
FMF GE-PAC 30 | FCF

DWG NO (FS40) 70B113006
CONT. ON SHEET 5 SH NO 4



MADE BY E. Ellwood JUN. 24 '69
ISSUED JUL 18 1969

APPROVAL E. G. White June 26, 69

DES.
CHKR. DR
REV. C

DWG NO (FS40) 70B113006
CONT ON SHEET 5 SH NO 4

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING				
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

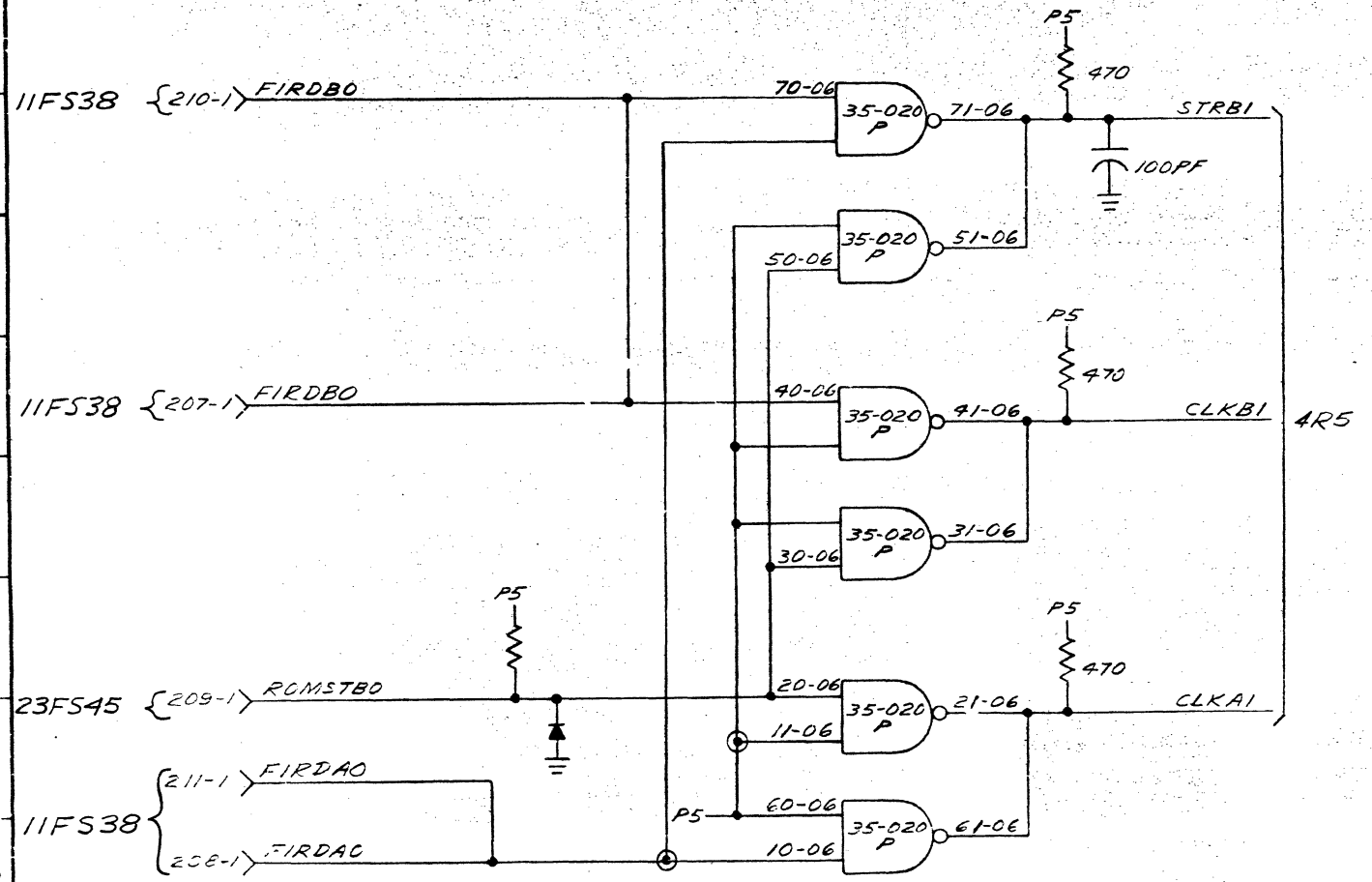
TITLE FUNCTIONAL SCHEMATIC
DROM TRANSFORMER
FMF GE-PAC 30 | FCF

DWG NO (FS40) 70B113006
CONT. ON SHEET 6 SH NO 5

A B C D E F G H J K L M N P R

2

STROBE LOGIC



MADE BY	APPROVAL	DES.	REV.
E. Ellsworth JUN. 24, '69	E.a. White June 26, 69		C
ISSUED JUL 18 1969		CHKR.	

DWG. NO (FS40) 70B113006
CONT ON SHEET 6 SH NO 5

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
DROM TRANSFORMER
FOR GE-PAC 30 1 FCF

DWG NO (FS40) 70B113006
CONT. ON SHEET 7 SH NO 6

BACK PANEL MAP

CONN POS	09																				
MOTH. BD	DRMT																				
VERT. POS	HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS				
	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2		
22		P5	GND																		
21	CRD000	CRD010																			
20	CRD020	CRD030																			
19	CRD040	CRD050																			
18	CRD060	CRD070																			
17	CRD080	CRD090																			
16	CRD100	CRD110																			
15	CRD120	CRD130																			
14	CRD140	CRD150																			
13	SRD140	SRD150																			
12	SRD120	SRD130																			
11	SRD100	SRD110	FIRDA7																		
10	SRD080	SRD090	FIRDB0																		
09	SRD060	SRD070	ROMSTB0																		
08	SRD040	SRD050	FIRDA0																		
07	SRD020	SRD030	FIRDB0																		
06	SRD000	SRD010	XS210																		
05	XS170	XS290	XS230																		
04	XS250	XS310	XS190																		
03	XS220	XS270	XS200																		
02	XS160	XS300	XS280																		
01	XS180	XS260	XS240																		
00		P5	GND																		
22		P5	GND																		
21																					
20	XS110	XS140	XS100																		
19	XS120	XS080	XS150																		
18	XS020	XS130	XS090																		
17	XS070	XS030	XS060																		
16	XS010	XS040	XS000																		
15	YS011	YS001	XS050																		
14	YS071	YS031	YS021																		
13	YS041	YS051	YS061																		
12	SRAL030	SRAL010	SRAL020																		
11	SRAH070	SRAL040	SRAL000																		
10	SRAL060	SRAH060	SRAL050																		
09	SRAH040	SRAL070	SRAH050																		
08	DXS110	DXS140	DXS020																		
07	DXS120	DXS150	DXS080																		
06	DXS090	DXS130	DXS100																		
05	DXS000	DXS060	DXS070																		
04	DYS010	DYS030	DXS040																		
03	DYS011	DYS001	DXS050																		
02	DYS071	DYS031	DYS021																		
01	DYS041	DYS051	DYS061																		
00		P5	GND																		

MADE BY G. Ellsworth JUN.24,'69
ISSUED JUL 18 1969
APPROVAL
DES.
CHKR. DR
REV C

DWG NO (FS40) 70B113006
CONT. ON SHEET 7 SH NO 6

DIP I.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:--

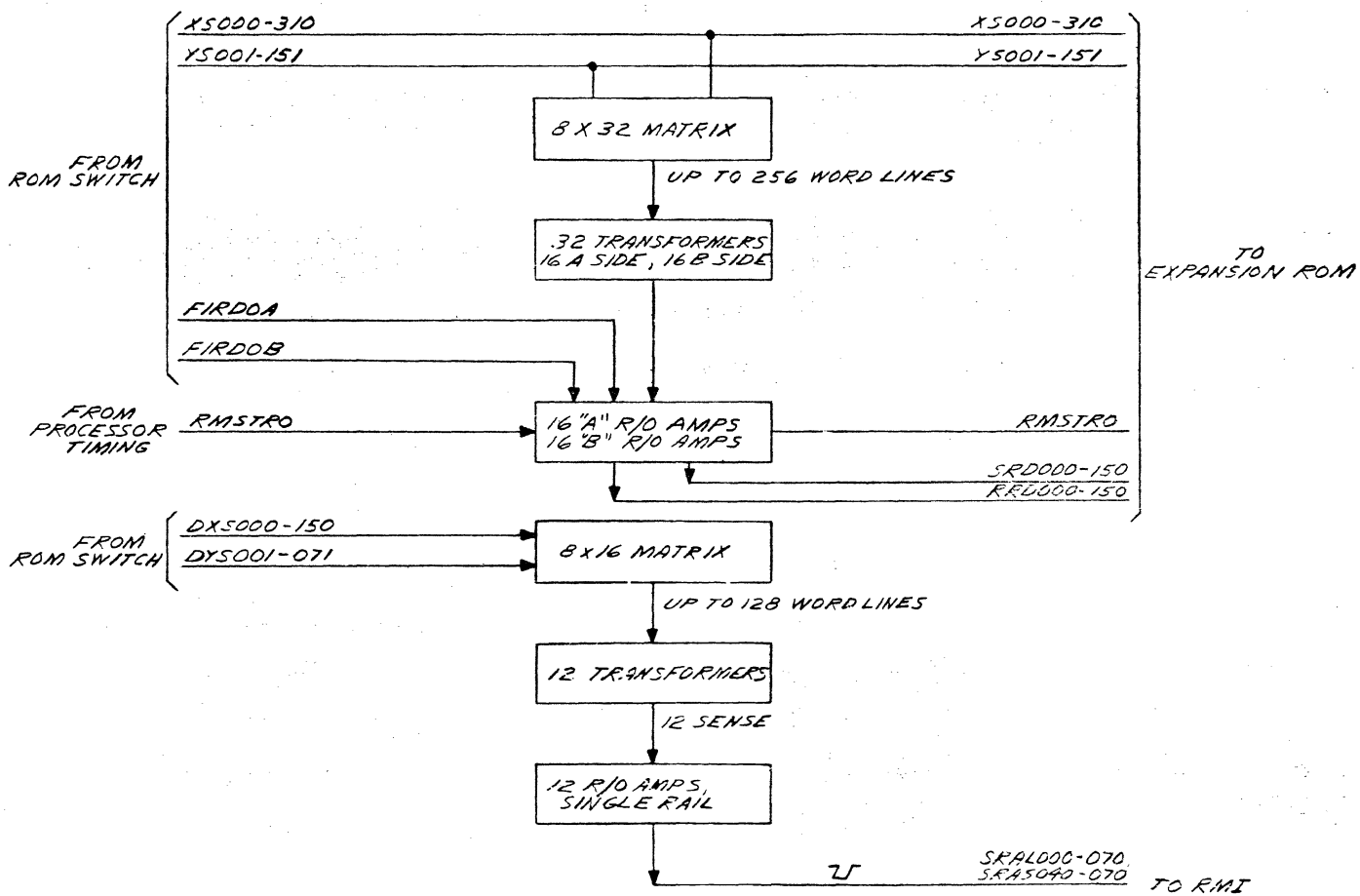
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS		
		FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
DROM TRANSFORMER
FMF GE-PAC 30 | FCF

DWG. NO (FS40)
70B113006
CONT. ON SHEET F SH. NO. 7

BLOCK DIAGRAM



MADE BY E. Edwards JUN. 24 '69
ISSUED JUL 18 1969

APPROVAL

DES.
CHKR. DR

REV. C

DWG. NO. (FS40)
70B113006
CONT ON SHEET F SH. NO. 7

GENERAL ELECTRIC

PROCESS COMPUTERS
PHOENIX ARIZONA

TITLE FUNCTIONAL SCHEMATIC
ROM INTERFACE

DRAWING NUMBER 70B113007 | CONT. 0A | PAGE 0

FIRST MADE FOR GE-PAC

(FS44)

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
C	ISSUED				

REISSUED

A	Issued										

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME

REISSUED

(FS44)

MADE BY E. Ellsworth JUN. 24, '69

APPROVAL OR S. A White June 26, 69

ISSUED July 18, 1969

REV. C

DWG. NO. 70B113007 | CONT. 0A | PAGE 0

PRINTS TO: K7-08

PCE 2981

DIST.	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:					GENERAL ELECTRIC	TITLE FUNCTIONAL SCHEMATIC	DWG NO (FS44)
	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES	PROCESS COMPUTER PHOENIX	ROM INTERFACE	70B113007
		√	±	±	±	FMF GE-PAC 30 1 PCF		CONT. ON SHEET 1 SH NO 0A

SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
SHEET INDEX SUPPORTING INFORMATION	0A	1	2																		
ROM DATA REGISTER	1	1	2																		
	2	1	2																		
	3	1	1																		
ROM ADDRESS LOWER REG.	4	1	1																		
	5	1	1																		
ROM ADDRESS HIGHER REG.	6	1	2																		
BACK PANEL MAP	7	1	1																		
	ISSUE DATE		1-31-69																		

SUPPORTING INFORMATION

CATEGORY	PART NO.
MOTHER BOARD ROM INTERFACE (RMIC)	35-092R02

SHEET INDEX NOTES:

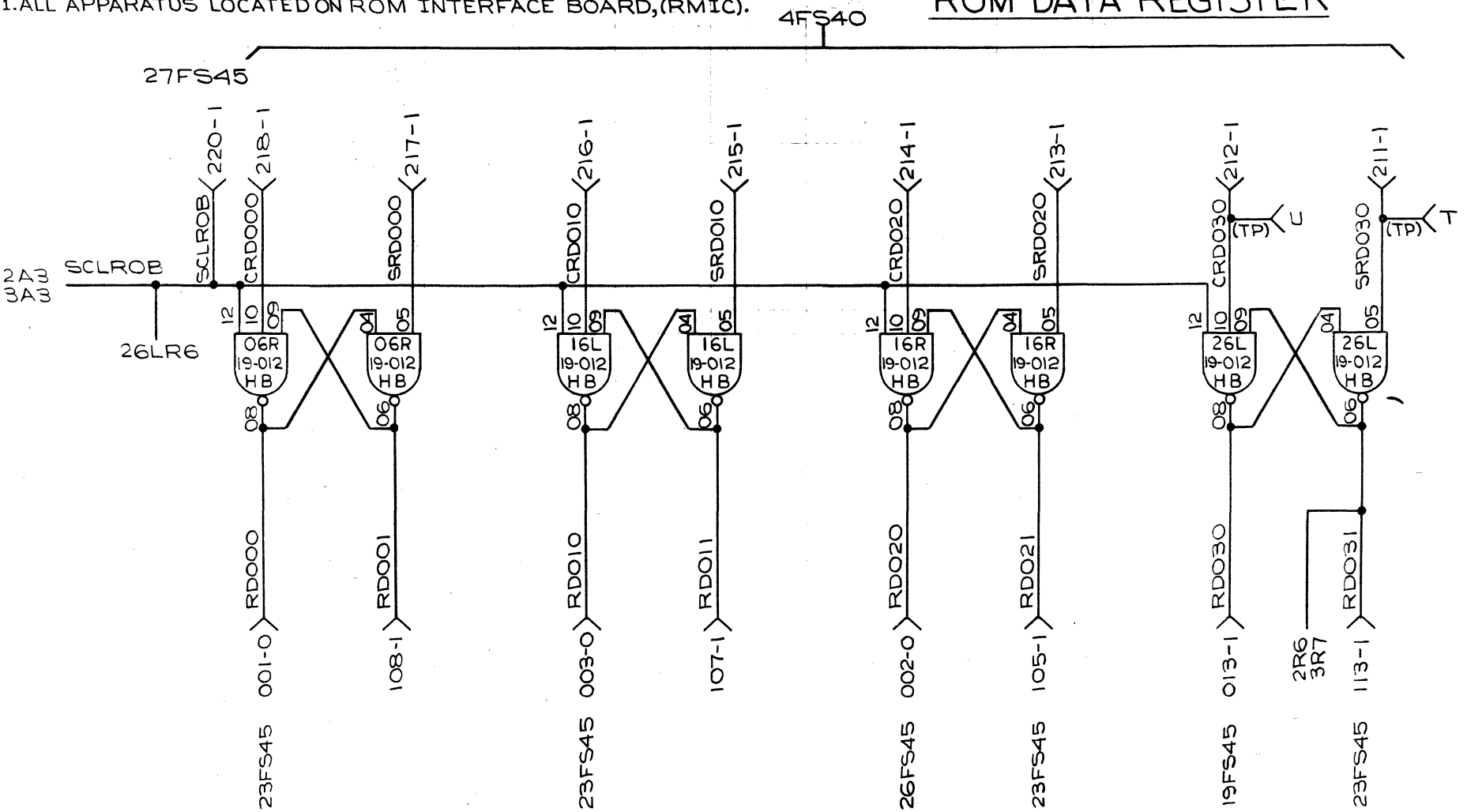
1. CHANGES ON THIS DRAWING SHALL REQUIRE ONLY THE REISSUE OF SHEETS AFFECTED.
2. THE ISSUE OF THIS SHEET SHALL DETERMINE THE LATEST ISSUE OF THIS DRAWING.

MADE BY	APPROVAL		REV.		DWG NO (FS44)
E. Ellsworth JUN. 24, '69	E. A. White June 25, 69	DES.	C		70B113007
ISSUED JUL 18 1969		CHKR.			CONT ON SHEET 1 SH NO 0A

DIST.	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—					GENERAL ELECTRIC	TITLE	DWG. NO. (FS44)
	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES	PROCESS COMPUTER PHOENIX	FUNCTIONAL SCHEMATIC ROM INTERFACE FMF GE-PAC 30 | FCF	70B113007 CONT. ON SHEET 2 SH. NO. 1
		V	±	±	±			

NOTES:
1. ALL APPARATUS LOCATED ON ROM INTERFACE BOARD, (RMIC).

ROM DATA REGISTER



MADE BY	APPROVAL	DES.	REV.		DWG. NO. (FS44)
C. Ellsworth JUL 3, 1969		CHKR.	C		70B113007
ISSUED JUL 18 1969					CONT ON SHEET 2 SH NO. 1

DIST.

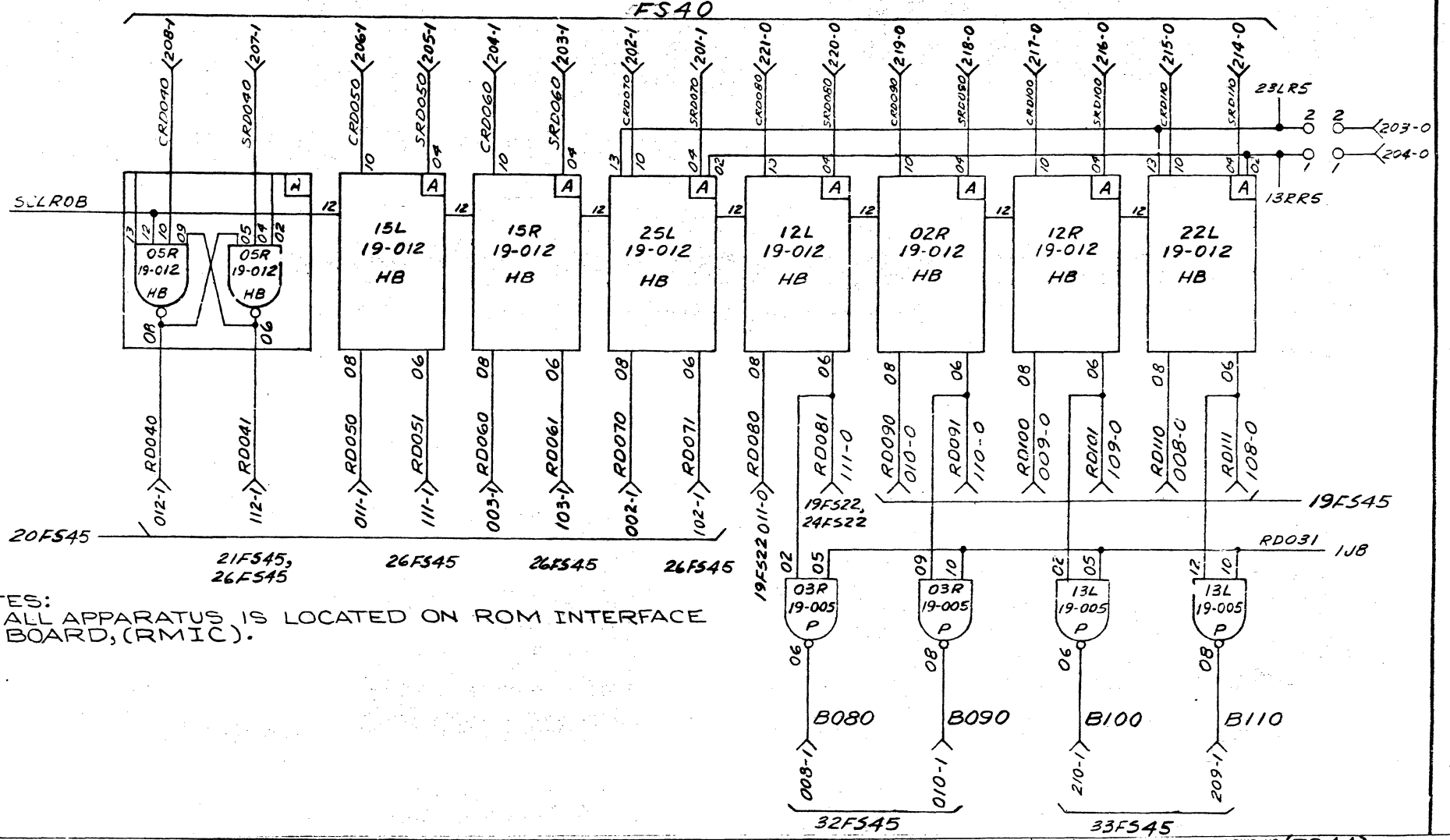
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES ✓ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGULAR ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
ROM INTERFACE
PMF GE-PAC 30 | FCF

DWG. NO. (FS44) 70B113007
CONT. ON SHEET 3 SH. NO. 2

ROM DATA REGISTER
FS40



NOTES:
1. ALL APPARATUS IS LOCATED ON ROM INTERFACE BOARD, (RMIC).

MADE BY	APPROVAL			
E. Ellsworth JUN. 24, 69	E.A. White June 25, 69	DES.	REV.	C
ISSUED JUL 18 1969		CHKR. GR		

DWG. NO. (FS44) 70B113007
CONT ON SHEET 3 SH NO. 2

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

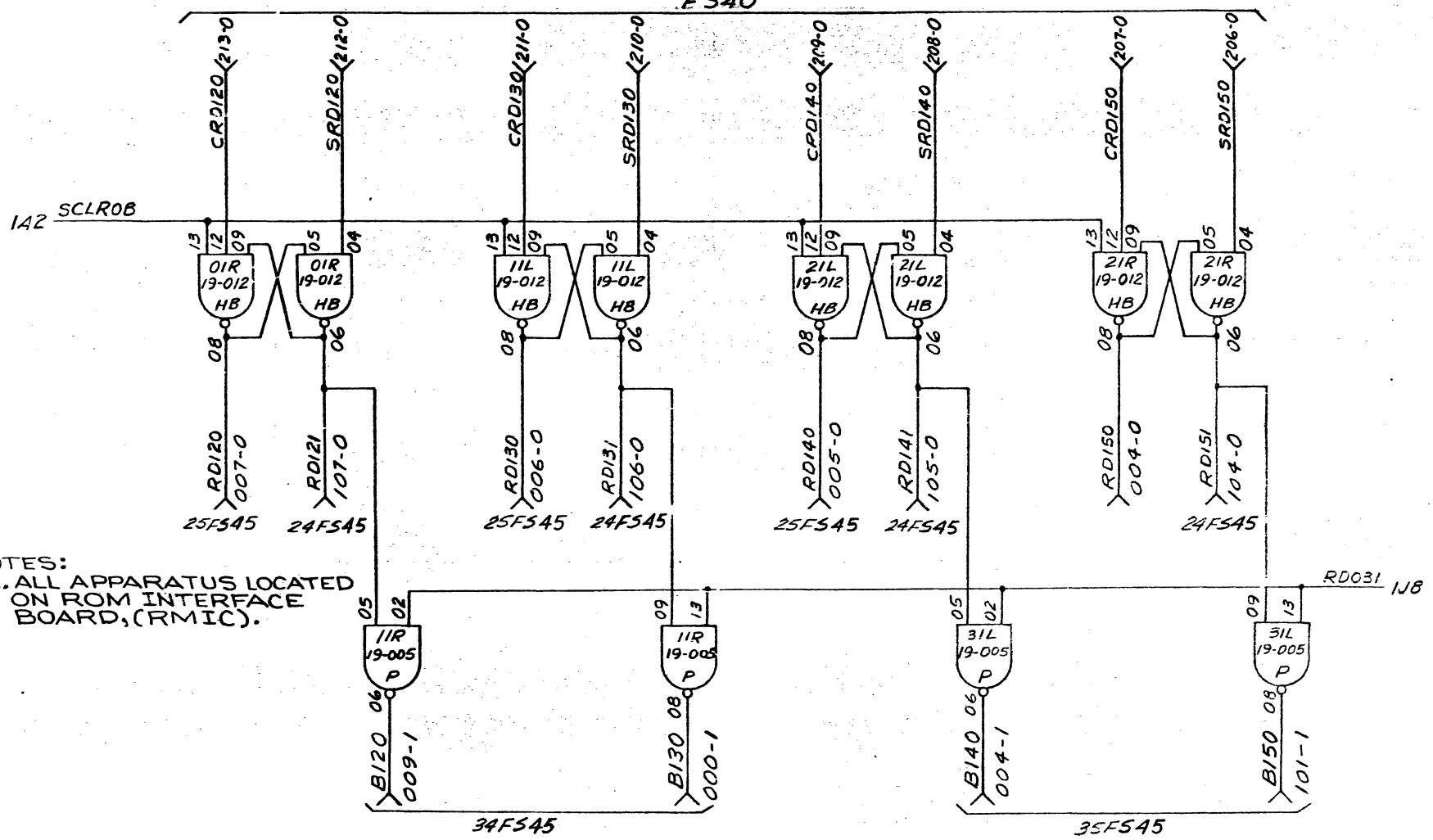
GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
ROM INTERFACE
FOR GE-PAC 30 1 FCF

DWG. NO. (FS44) 70B113007
CONT. ON SHEET 4 SH. NO. 3

ROM DATA REGISTER

FS40



NOTES:
1. ALL APPARATUS LOCATED ON ROM INTERFACE BOARD, (RMIC).

MADE BY E. Ellsworth JUN. 24, 69
JUL 18 1969

APPROVAL E.A. White June 25, 69

DES. | CHKR. DR | REV. C

DWG NO. (FS44) 70B113007
CONT ON SHEET 4 SH NO. 3

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:--
APPLIED PRACTICES | SURFACES: V | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
ROM INTERFACE
FMF GE-PAC 30 | 1 FCF

DWG. NO (FS44)
70B113007
CONT. ON SHEET 5 SH. NO. 4

ROM ADDRESS LOWER REGISTER

1

NOTES:
1. ALL APPARATUS IS LOCATED ON ROM INTERFACE BOARD, (RMIC).

MADE BY E. Ellsworth JUN. 23, '69
ISSUED JUL 18 1969

APPROVAL E. A. White June 25, 69

DES.
CHKR. OR
REV. C

DWG. NO. (FS44)
70B113007
CONT ON SHEET 5 SH. NO. 4

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES ✓ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
ROM INTERFACE
FMF GE-PAC 30 | FCF

DWG. NO. (FS44) 70B113007
CONT. ON SHEET 6 SH. NO. 5

ROM ADDRESS LOWER REGISTER

33F545 32F545

1

4R4 WUN1
4R6 RALCA1
4A4 LRALO
4C1 LRALIA
4R5 SCLRQA
4N9 RCLI1

37R 19-003 G
34R 19-002 G
44L 19-001 G
25R 19-003 G
45R 19-003 G
35R 19-003 G
35L 19-014 T FF J DS 1
45L 19-014 T FF J DS 1

44LD2

35LR6 4.7K P5
34LR6 4.7K P5
45LR5 4.7K P5
44LR5 4.7K P5

S111 019-1
S101 020-1
S091 021-1
S081 022-1

SRALO30 017-0
RALO30A 117-1
SRALO20 012-0
RALO20A 120-1
SRALO10 000-0
RALO10A 118-1
SRALOOO 102-0
RALOOOA 121-1
NC

NOTES:
1. ALL APPARATUS IS LOCATED ON ROM INTERFACE BOARD, (RMIC).

MADE BY G. Ellsworth JUN. 24, '69
APPROVAL E. A White June 25, 69
JUL 18 1969
DES.
CHKR. DR
REV. C

DWG. NO. (FS44) 70B113007
CONT ON SHEET 6 SH NO. 5

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS, DECIMALS, ANGLES

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
ROM INTERFACE
FOR GE-PAC 30 | PCF

DWG. NO. (FS44) 70B113007
CONT. ON SHEET 7 SH. NO. 6

ROM ADDRESS HIGHER REGISTER

2

4A7 RCLO
BANK1 007-1
LRAHO 006-1
4A4 LRALO
4R5 SCLROA
22FS45
24FS45

41L 19-005 P
41R 19-005 P
40R 19-005 P
42LR1 P5 470
40RR2 P5 470
D (TP)
(TP) B

4D1 S071
4G1 S061
4K1 S051
4P1 S041

31R 19-003 G
40L 19-003 G
30R 19-003 G
20L 19-003 G

30L 19-014 FF
20R 19-014 FF
K T J DC DS 0 1 N.C.

22RR1 P5 4.7K
31RR5 P5 4.7K
20RR2 P5 4.7K
21RR1 P5 4.7K

RAH070A 119-1
SRAH070 018-1
RAH060A 110-1
SRAH060 221-1
RAH050A 116-1
SRAH050 101-0
RAH040A 109-1
SRAH040 205-0
1FS3

NOTES:
1. ALL APPARATUS LOCATED ON ROM INTERFACE BOARD, (RMIC).

MADE BY E. Ellsworth JUN. 24, '69
ISSUED JUL 18 1969
APPROVAL E.G. [illegible] June 25, 69
DES.
CHKR. DR
REV. C

DWG. NO. (FS44) 70B113007
CONT ON SHEET 7 SH NO. 6

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --
APPLIED PRACTICES | SURFACES √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
ROM INTERFACE
FOR GE-PAC 30 | FCP

DWG NO (FS44) 70B11300
CONT. ON SHEET F SH NO 7

BACK PANEL MAP

CONN POS		10																
MOTH. BD		RMI																
VERT. POS		HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS		
		0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2
1	22	S001	P5	GND															
	21	S011	RAL000	SRAH060															
	20	S021	RAL020	SCLR0B															
	19	S031	RAH070	INHINC															
	18	SRAH070	RAL010	CRD000															
	17	DRD001	RAL030	SRD000															
	16	DRD000	RAH050	CRD010															
	15	DRD010	DRD011	SRD010															
	14	DRD020	DRD021	CRD020															
	13	RD030	RD031	SRD020															
	12	RD040	RD041	CRD030															
/	11	RD050	RD051	SRD030															
	10	B010	RAH060	B020															
	09	B040	RAH040	B030															
	08	B000	RD001	CRD040															
	07	BANK1	RD011	SRD040															
	06	LRAH0	LRAL0	CRD050															
	05	SRAL040	RD021	SRD050															
	04	B060	RCL0	CRD060															
	03	RD060	RD061	SRD060															
	02	RD070	RD071	CRD070															
	01	SCLR0A	B070	SRD070															
	00	B050	P5	GND															
0	22	S041	P5	GND															
	21	S051	SRAL050	CRD080															
	20	S061	SCLR1	SRD080															
	19	S071	RAL040	CRD090															
	18	SRAL060	RAL050	SRD090															
	17	SRAL030	RAL060	CRD100															
	16	SRAL000	RAL070	SRD100															
	15	DF010	DF001	CRD110															
	14	DF020	DF011	SRD110															
	13		DF021	CRD120															
	12	SRAL020	DF031	SRD120															
	11	RD080	RD081	CRD130															
	10	RD090	RD091	SRD130															
	09	RD100	RD101	CRD140															
	08	RD110	RD111	SRD140															
	07	RD120	RD121	CRD150															
	06	RD130	RD131	SRD150															
	05	RD140	RD141	SRAH040															
	04	RD150	RD151	DF071															
	03	RD010	SRAL070	DF061															
	02	RD020	SRAL000	DF051															
	01	RD000	SRAH050	DF041															
	00	SRAL010	P5	GND															

MADE BY E. Ellsworth JUN. 24, '69
ISSUED JUL 18 1969

APPROVAL E. A. White June 25, 69

DES. | CHKR. OK | REV. C

DWG. NO. (FS44) 70B113007
CONT ON SHEET F SH NO. 7

GENERAL ELECTRIC

PROCESS COMPUTERS
PHOENIX ARIZONA

TITLE

FUNCTIONAL SCHEMATIC PROCESSOR (MOD 30-2)

DRAWING NUMBER 70B113008 | CONT. 0A | PAGE 0

FIRST MADE FOR GE-PAC 30

(FS 45)

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
E	ISSUED				

REISSUED

E Issued

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME

REISSUED

(FS 45)

MADE BY	APPROVAL	REV		DWG. NO.	CONT.	PAGE
K. Kotzin JUNE 24/69	E. G. White June 25, 69	E		70B113008	0A	0
ISSUED July 18, 1969				PRINTS TO: K7-08		

PCE 2081

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE: FUNCTIONAL SCHEMATIC PROCESSOR (MOD 30-2)
PWF: GE-PAC 30 | FCF

DWG NO (FS 45) 70B113008
CONT ON SHEET | SH NO

SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
CLOCK CONTROL	22	1	2	2	2																
CLOCK GENERATORS	23	1	2	2	2																
I/O CONTROL	24	1	2	2	2																
	25	1	2	2	2																
ARITHMETIC CARRY CKT	26	1	2	2	2																
ARITHMETIC LOGIC UNIT	27	1	2	2	2																
	28	1	2	2	2																
BACK PANEL MAP	29	1	1	1	1																
	30	1	1	1	1																
BLOCK DIAGRAM	31	1	1	1	1																
ISSUE DATE		8-27-69	12-11-69	4-3-69	4-3-69																

SUPPORTING INFORMATION

CATEGORY	PART NO.

SHEET INDEX NOTES:

1. CHANGES ON THIS DRAWING SHALL REQUIRE ONLY THE REISSUE OF SHEETS AFFECTED.
2. THE ISSUE OF THIS SHEET SHALL DETERMINE THE LATEST ISSUE OF THIS DRAWING.

MADE BY	APPROVAL	DES.		REV.	
Kathy Ieaf JUNE 24, '69	E. A. White June 25, 69	CHKR	DP		E

ISSUED: JUL 18 1969

DWG. NO. (FS 45) 70B113008
CONT ON SHEET | SH NO. C

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:-- | APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ±, DECIMALS ±, ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE: FUNCTIONAL SCHEMATIC
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

DWG NO (FS45) 70B113008
CONT. ON SHEET 2 SH NO.

2

A REGISTER & INSTRUCTION REGISTER

BIT SLICE																							
3	13	15			15			14			14			13			13			12			12
2	11				11			10			10			09			09			08			08
1	07				07			06			06			05			05			04			04
0	03				03			02			02			01			01			00			00

2B5, 3K4, 27D8, 27H8, 27K8, 27R8, 28D8, 28H8, 28K8, 28R8

5A9, 13A4, 25R3 > CLOD 001-1

15LD1

10F9 LARO 206-1
9N8 UIRO 103-1
10E9 LIRO 108-1

14L 19-012 HB
44R 19-003 G
15L 19-016 HG
44R 19-003 G

14R 19-012 HB
25L 19-007 R T S 0 FF 1
25R 19-007 R T S 0 FF 1
35L 19-007 R T S 0 FF 1
35R 19-007 R T S 0 FF 1
24L 19-007 R T S 0 FF 1
24R 19-007 R T S 0 FF 1
34L 19-007 R T S 0 FF 1
34R 19-007 R T S 0 FF 1

8E9 > UAI 104-1

15L 19-016 HG
36L 19-003 G
36L 19-003 G
36L 19-003 G
36L 19-003 G
26L 19-005 P
26R 19-005 P
26L 19-005 P
26R 19-005 P

S__1 > 203-1
GA__0 > 28J2
AR__1 > 221-1
2BB2
GA__0 > 221-0 > 18N9
AR__1 > 220-1
GA__0 > 27J2
AR__1 > 219-1
GA__0 > 27B2
AR__1 > 218-1

B__0 > 3J8, 26C7, 28K2
IR__1 > 210-1 > 8P1, 8R1, 16L1, 16R1
B__0 > 3J8, 26C6, 28E2
IR__1 > 209-1 > 8J1, 8N1, 16P1
B__0 > 3J8, 26C9, 27K2
IR__1 > 208-1 > 8H1, 8M1, 16K1, 16N1
B__0 > 3J8, 26C8, 27E2
IR__1 > 207-1 > 8H1, 8K1, 16M1

BIT SLICE																							
3	13	15			15			14			14			13			13			12			12
2	11				11			10			10			09			09			08			08
1	07				07			06			06			05			05			04			04
0	03				03			02			02			01			01			00			00

NOTE: 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON BIT SLICE BDS 0, 1, 2 & 3.

MADE BY R. Katayama JUNE 24, '69
ISSUED JUL 18 1969
APPROVAL E. A. White June 25, 69
DES.
CHKR. DR
REV. E

DWG. NO. (FS45) 70B113008
CONT ON SHEET 2 SH NO. 1

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING —
APPLIED PRACTICES | SURFACES √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

DWG NO (FS45)
70B113008
CONT. ON SHEET 3 SH NO 2

USER REGISTER STACK

BIT SLICE				
3	12	13	14	15
2	08	09	10	11
1	04	05	06	07
0	00	01	02	03

BIT SLICE				
0	1	2	3	
00	04	08	12	
01	05	09	13	
02	06	10	14	
03	07	11	15	

IM2

S--1 34RPS 220 51-04
S--1 34LRS 220 41-04
S--1 24RPS 220 31-04
S--1 24LRS 220 21-04

P/O 35-041
40-04
30-04
20-04
10-04
50-05
P5

IIN3
9N2

P5
01L 19-009
00L 19-009

13L 12L 01R 00R 11L 10L

A B C D E F G H
3A5

NOTE: 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON BIT SLICE BOARDS 0, 1, 2 & 3.

MADE BY J. Katajisalo, JUNE 24, 69
ISSUED JUL 18 1969
APPROVAL E.G. White June 25, 69
DES.
CHKR. DR
REV. E

DWG. NO. (FS45) 70B113008
CONT ON SHEET 3 SH NO. 2

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

DWG. NO. (FS45) 70B113008
CONT. ON SHEET 4 SH NO. 3

MICRO REGISTER STACK

BIT SLICE									
3	MR2	LOC	MR3	MAR		MR1	MAR	MR3	GND
2	MR3	PSW	MR2	LOC		MR0	MR3	MR1	MAR
1	MR1	MAR	MR3	PSW		MR1	LOC	MR0	MR4
0	MR0	MR4	MR1	MAR		MR3	PSW	MR2	LOC

IO INPUT/OUT

BIT SLICE									
3	15			14		07			06
2	13			12		05			04
1	11			10		03			02
0	09			08		01			00

07L 19-009
06L 19-009
07R
06R
17L 19-005 P
16L 19-005 P
17LRS 1K
17LR2 1K
16LRS 1K
16LR2 1K
36RRS PS 220
36LRS PS 220
26RRS PS 220
26LRS PS 220
27R 19-005 P
46L 19-004
46R 19-005 P
46LRS PS 180
27RRS
27RR2

NOTE: 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON BIT SLICE BOARDS 0, 1, 2 & 3.

1J8, 1L8, 1N8, 1P8

BIT SLICE																					
3	MR2	LOC	MR3	MAR		MR1	MAR	MR3	GND		15	14	13	12		07		06		15	14
2	MR3	PSW	MR2	LOC		MR0	MR3	MR1	MAR		11	10	09	08		05		04		13	12
1	MR1	MAR	MR3	PSW		MR2	LOC	MR0	MR4		07	06	05	04		03		02		11	10
0	MR0	MR4	MR1	MAR		MR3	PSW	MR2	LOC		03	02	01	00		01		00		09	08

MADE BY Katajack JUNE 24, 69
ISSUED JUL 16 1969
APPROVAL E. G. White JUNE 25, 69
DES.
CHKR. OR
REV. E

DWG. NO. (FS45) 70B113008
CONT ON SHEET 4 SH NO. 3

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS		
		FRACTIONS	DEC. HALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

DWG. NO. (FS45)
70B113008
CONT. ON SHEET 5 SH. NO. 4

A B C D E F G H J K L M N P R

1 2 3 4 5 6 7 8 9

2

FLAG REGISTER

SHRI 2782 213-0 B150 6P9
SHLI 2762 021-0 B000 2702 215-0
CSVI 2643 008-1 SVACI 1689 201-1 2046
CO01 2695 000-0 CSVO 208-1 2064
1A8
S1251 (205-1) S811: (204-1) S047! (203-1) S0031 (202-1) FLR150 5N9 FLR140 5L9
STF! 5A1
S001 (211-1)
TTESTO 1287 117-0 CTST1 1549 017-1
TTEST! 1286 017-0
DO 1649 110-0 U00D 111-0

51-37 71-37 35-060 G
60-07 35-115 HG 70-07
50-07 35-115 HG 40-07
51-04 41-04 61-04 71-04 11-04 21-04 31-04 10-04 20-04 30-04 40-04 50-04
35-022 P 60-04
70-37 35-060 G 60-37
30-07 35-115 HG 20-07
71-41 35-060 G 61-41

STFI

60-25 70-25 35-001 G 50-25
61-35 71-35 35-001 G 51-35
31-35 41-35 35-001 G 21-35
30-34 40-34 50-34 35-002 G 20-34
51-34 41-34 31-34 35-002 G 21-34
30-35 40-35 35-001 G 20-35
60-35 70-35 35-001 G 50-35
60-36 10-36 35-020 P 61-36
70-36 35-020 P 71-36
71-40 61-40 35-116 HG 51-40

SFL120 221-1 5H1
SFL130 220-1 5K1
GF1451 5E1
SFL140 219-1 5M1
SFL150 218-1 5P1
LRAH10 109-0

NOTE: 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON CONTROL 2 BD (C02).

MADE BY J. Katajisto JUNE 24 '69
APPROVAL S. G. White June 25, 69
ISSUED JUL 18 1969

DES.
CHKR DR
REV. E

DWG. NO. (FS45)
70B113008
CONT ON SHEET 5 SH. NO. 4

DIST.

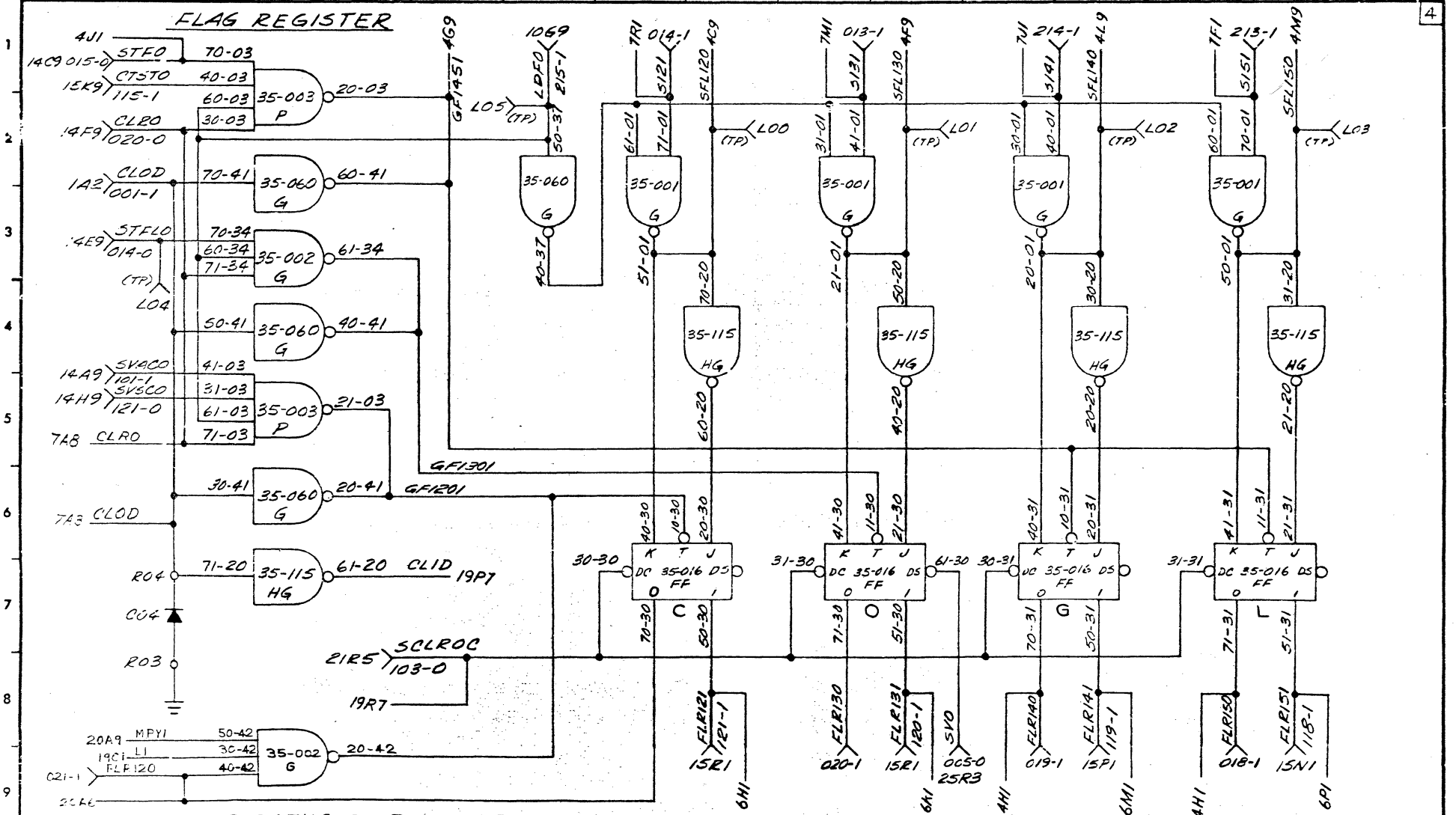
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING ---
APPLIED PRACTICES | SURFACES: V | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± . DECIMALS ± . ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE: FUNCTIONAL SCHEMATIC
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

DWG NO. (FS45) 70B113008
CONT. ON SHEET 6 SH NO 5

FLAG REGISTER



NOTE: 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON CONTROL 2 BD (CO2).

MADE BY J. Katajisto JUNE 24, 69
APPROVAL E. A. White June 25, 69
ISSUED JUL 18 1969
DES.
CHKR. DR
REV. E

DWG. NO. (FS45) 70B113008
CONT ON SHEET 6 SH NO. 5

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING: —

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

DWG. NO. (FS 45)
70B113008
CONT. ON SHEET 7 SH. NO. 6

CONDITION CODE REGISTER

9N7 UPSWO 004-1 30-37 → 35-060 G → 2C-37 → (TP) LO7

14G9 LCCO 002-1 91-07 → 35-115 HG → 21-07 → 41-32, 40-33

35-009

5H9 FLR121: 71-33, 41-33
5K9 FLR131: 31-33
5M9 FLR141: 71-32, 40-32
5P9 FLR151: 31-32

51-33, 61-33, 11-33, 21-33, 51-32, 61-32, 11-32, 21-32

G, G, G, G, P

A, A, A, A

60-33, 70-33, 20-33, 10-33, 60-32, 70-32, 20-32, 10-32

B120 50-33 → 115-0
B130 30-33 → 114-0
B140 50-32 → 113-0
B150 30-32 → 112-0
2D9 A1

NOTE: 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON CONTROL 2 BD (CO2).

2

1

MADE BY	APPROVAL	DES.		REV.	E
J. Katajisto JUNE 24, 69	E. G. White June 25, 69	CHKR.	DR		
ISSUED JUL 18 1969					

DWG. NO. (FS 45) 70B113008
CONT ON SHEET 7 SH. NO. 6

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

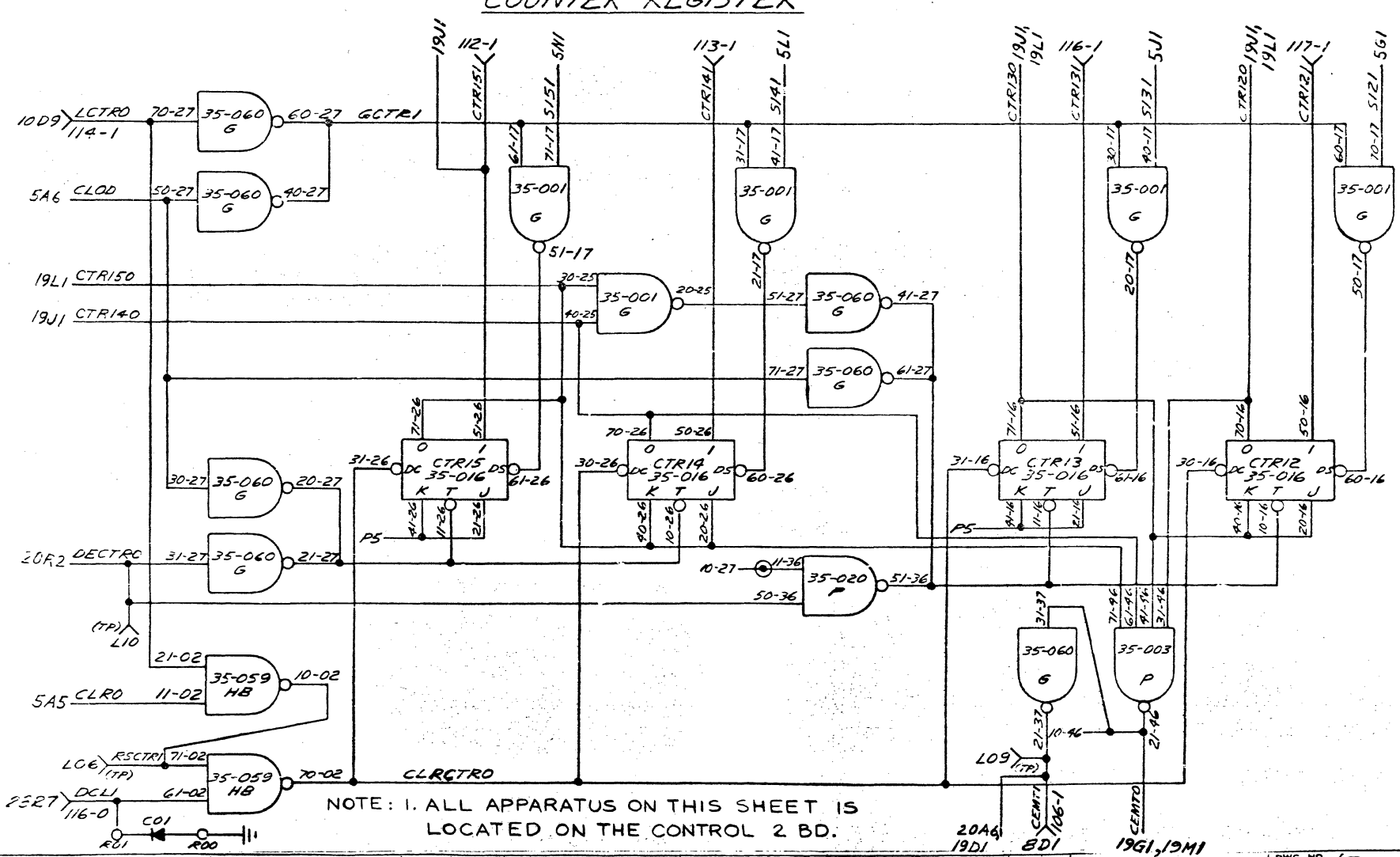
GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

DWG NO. (FS45) 70B113008
CONT. ON SHEET 8 SH NO 7

COUNTER REGISTER

2



NOTE: 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON THE CONTROL 2 BD.

MADE BY J. Katajineb, JUNE 24,69
ISSUED JUL 18 1969
APPROVAL E. G. White June 25, 69
DES.
CHKR. DR
REV. E

DWG. NO. (FS45) 70B113008
CONT ON SHEET 8 SH NO. 7

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE: FUNCTIONAL SCHEMATIC
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

DWG NO (FS45)
70B113008
CONT. ON SHEET 9 SH NO 8

SOURCE DECODE

YD / YS

2

NOTE: 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON THE CONTROL ϕ BD.

PART OF DESTINATION DECODING (YD OR YS)

N.C.

MADE BY J. Ratajack, JUNE 24, 69
ISSUED JUL 18 1969

DES. E. a White June 25, 69
CHKR. DR

REV. E

DWG. NO. (FS45) 70B113008
CONT ON SHEET 9 SH NO. 8

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING —
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE: FUNCTIONAL SCHEMATIC
PROCESSOR (MOD 30-2)
FMS: GE-PAC 30 | FCF

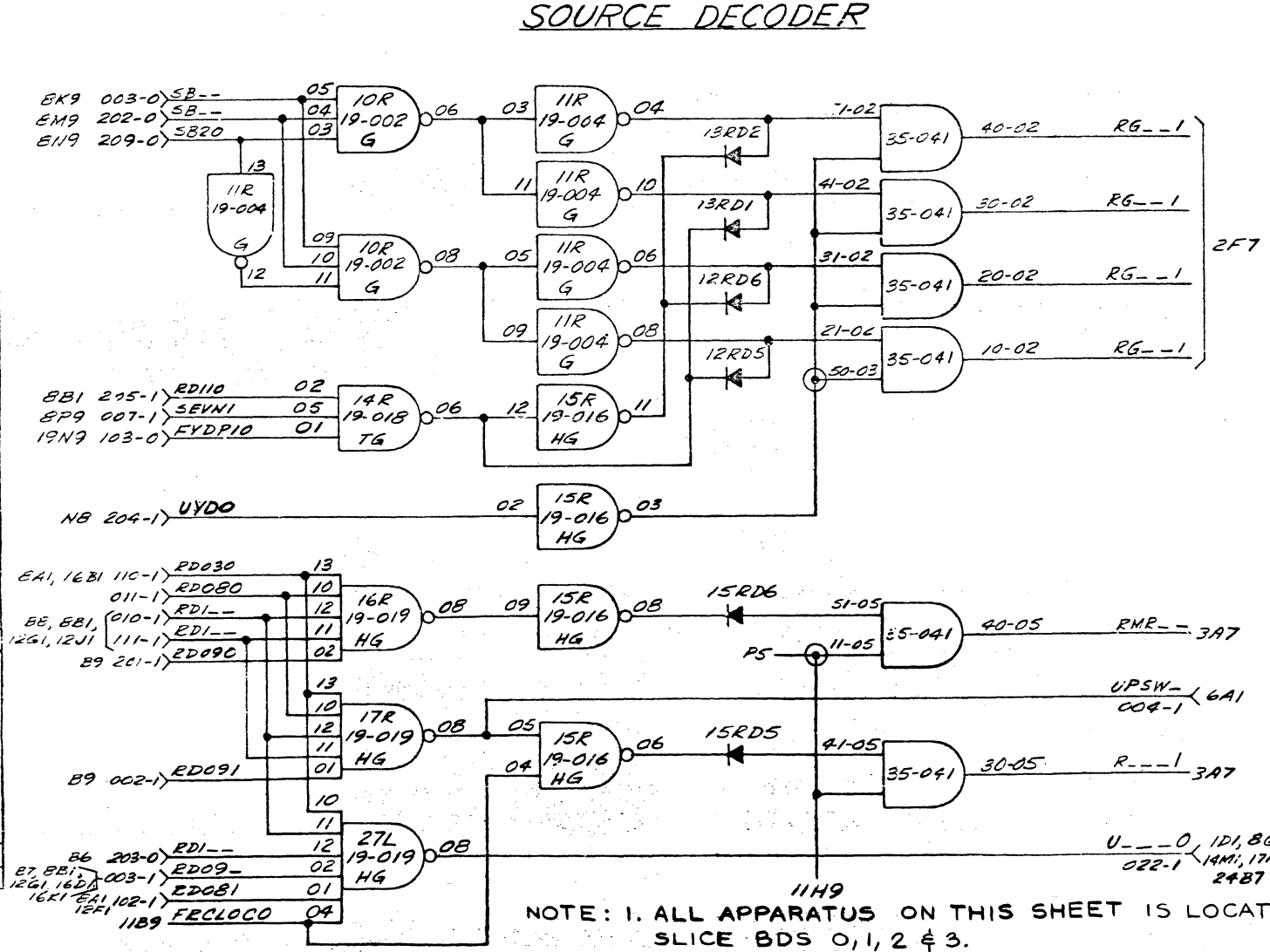
DWG NO (FS45) 70B113008
CONT. ON SHEET 10 SH. NO. 9

SOURCE DECODER

2

BIT SLICE			
0	1	2	3
00	00	01	01
10	11	10	11

BIT SLICE			
0	1	2	3
00	04	08	12
01	05	09	13
02	06	10	14
03	07	11	15
01	11	31	21
NC	NC	0	NC
MR4	MAR	PSW	LOC
IR	IR4	IO	YD



NOTE: 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON BIT SLICE BDS 0, 1, 2 & 3.

MADE BY J. Katajisto JUNE 24, 69
ISSUED JUL 18 1969
APPROVAL E. A. White June 25, 69
DES.
CHKR. DR
REV. E

DWG. NO. (FS45) 70B113008
CONT ON SHEET 10 SH NO. 9

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

DWG. NO. (FS45)
70B113008
CONT. ON SHEET 11 SH. NO. 10

DESTINATION DECODER

NOTE:
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON CONTROL O BD (COϕ).

MADE BY J. Katajisek, JUNE 24, 69
ISSUED JUL 18 1969
APPROVAL E.G White June 25, 69
DES.
CHKR. DR
REV. E

DWG. NO. (FS45)
70B113008
CONT ON SHEET 11 SH NO. 10

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± . | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

DWG NO (FS 45) 70B113008
CONT. ON SHEET 12 SH NO 11

DESTINATION DECODER

BIT SLICE			
0	1	2	3
00	00	01	01
10	11	10	11
0	0	GND	0
0	0	1	1
0	1	1	0
NC	NC	NC	C

BIT SLICE			
0	1	2	3
CC	C4	CE	12
01	05	09	13
02	06	10	14
03	07	11	15
0	1	3	2
0	1	3	2
MRG	MAR	PSW	LOC

8F9 218-0 ENG1
10M9 217-0 DB--
216-0 DB--
215-0 DB20
10R1, 19N9 102-0 DEVN1
27R7 002-0 STCLK0
13H9 219-0 BANK—
10H1, 20R4 120-0 GRD040
10A5 208-0 RDO50
10A2, 12D1, 220-0 RDO6—
15N1
10A3, 12E1, 121-0 RDO7—
15N1, 19N1
16J9 989 FRCLOC— 202-1

12R 19-001 G
13R 19-004 G
10R 19-002 G
11R 19-004 G
47L 19-001 G
35-041

14RD2, 14RD1, 13RD6, 13RD5
03LD4, 03LD5, 04LD1, 03LD6, 04LD2
15RR2 4.7K PS
9J9

40-03 WG--1
30-03 WG--1
20-03 WG--1
10-03 WG--1
2F3
20-05 WMR-1
10-05 W---1
3A3
U0-0 020-0 4R1, 10L1 22A3

LOSTK1

NOTE: 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON BIT SLICE BDS 0, 1, 2 & 3.

MADE BY J. Ratajack JUNE 24, '69
ISSUED JUL 18 1969
DES. E. A. White June 25, 69
CHKR. DR
REV. E

DWG. NO. (FS 45) 70B113008
CONT ON SHEET 12 SH NO. 11

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:--

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

DWG NO (FS 45)
70B113008
CONT. ON SHEET 13 SH NO 12

TEST CONTROL

3

NOTES:
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON THE CONTROL 3 BD.
2. OPTIONAL EQUIPMENT SUPPLY ONLY AT CUSTOMERS REQUEST.

SEE NOTE 2

MADE BY J. Katajack JUNE 24, 69
ISSUED JUL 18 1969

APPROVAL E. A White June 25, 69

DES.
CHKR. DR

REV. E

DWG. NO. (FS 45)
70B113008
CONT ON SHEET 13 SH NO. 12

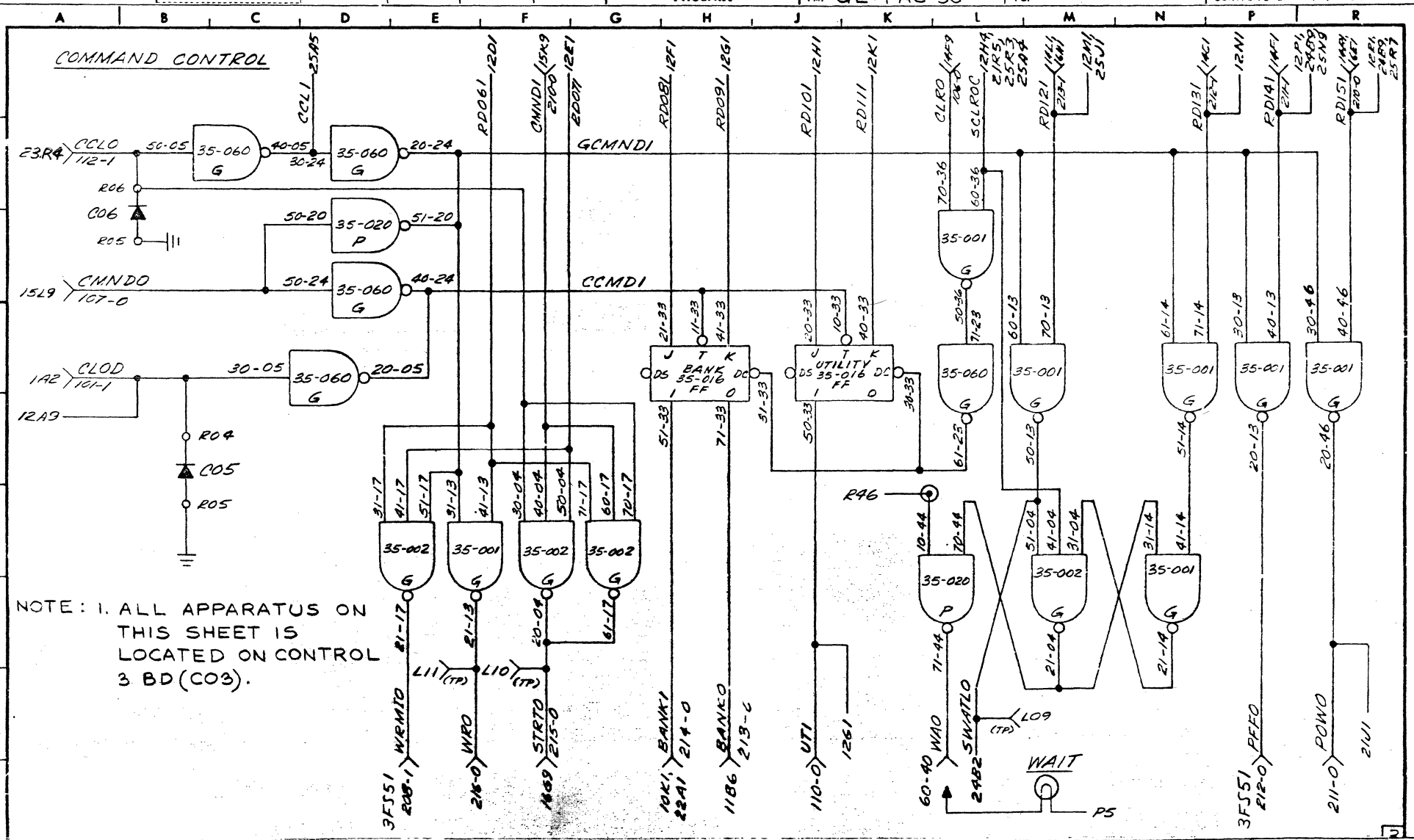
DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±
SURFACES: √

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE: FUNCTIONAL SCHEMATIC PROCESSOR (MOD. 30-2)
FMF GE-PAC 30 1 FCF

DWG NO (FS 45) 70B113008
CONT. ON SHEET 14 SH NO 13



NOTE: 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON CONTROL 3 BD (C03).

MADE BY J. Ratajick JUNE 24, 69
ISSUED JUL 18 1969

APPROVAL E.A. White June 25, 69

DES.
CHKR. DR

REV. E

DWG. NO. (FS 45) 70B113008
CONT ON SHEET 14 SH NO. 13

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

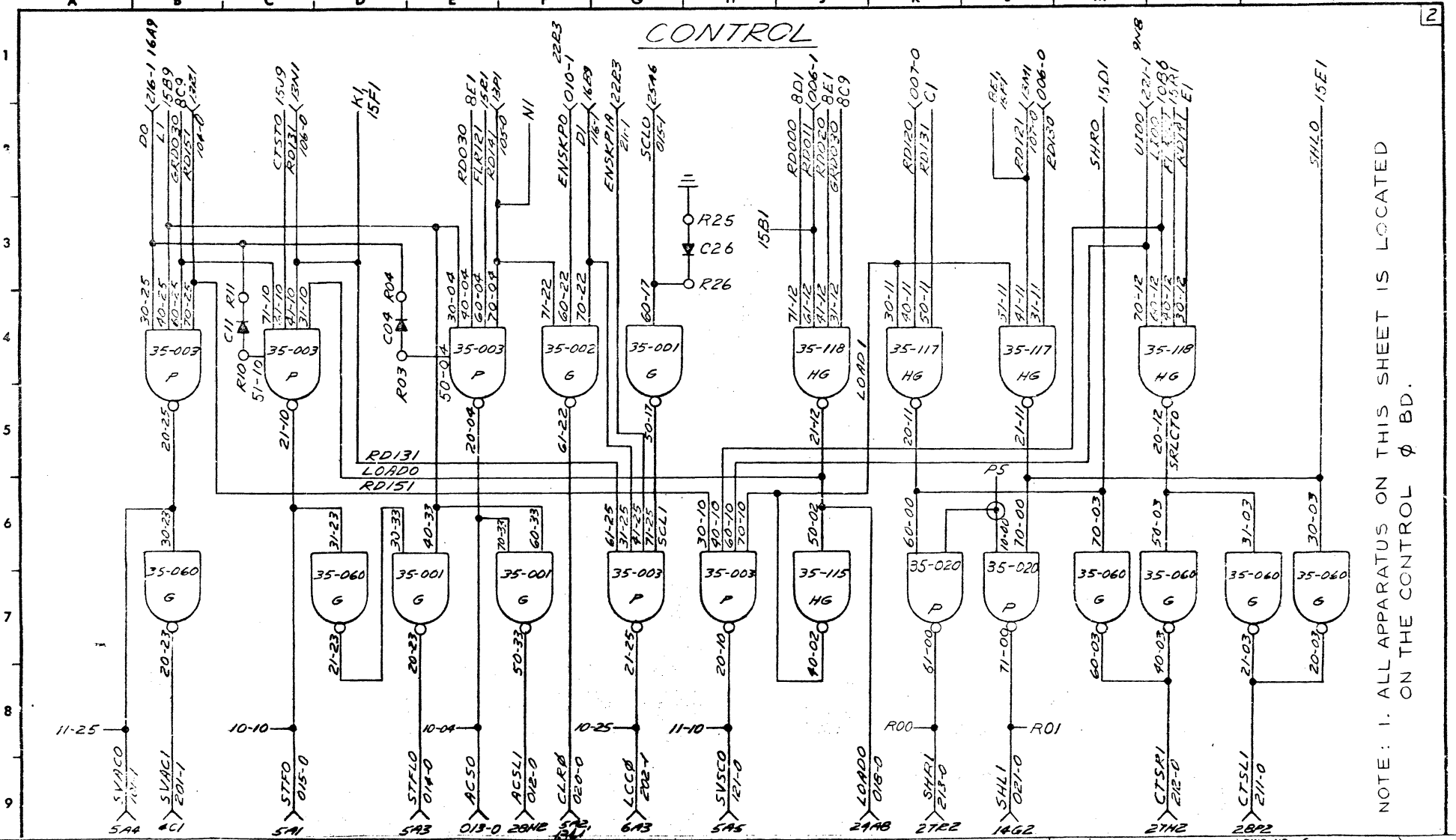
TITLE: FUNCTIONAL SCHEMATIC
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

DWG NO (FS 45)
70B113008
CONT. ON SHEET 15 SH NO 14

CONTROL

2

NOTE: 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON THE CONTROL Ø BD.



MADE BY J. Katajisto JUNE 24, 69
APPROVAL E.G. White June 25, 69
ISSUED JUL 18 1969
DES. DR CHKR.
REV. E

DWG. NO. (FS 45) 70B113008 CONT ON SHEET 15 SH NO 14

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±
SURFACES: √

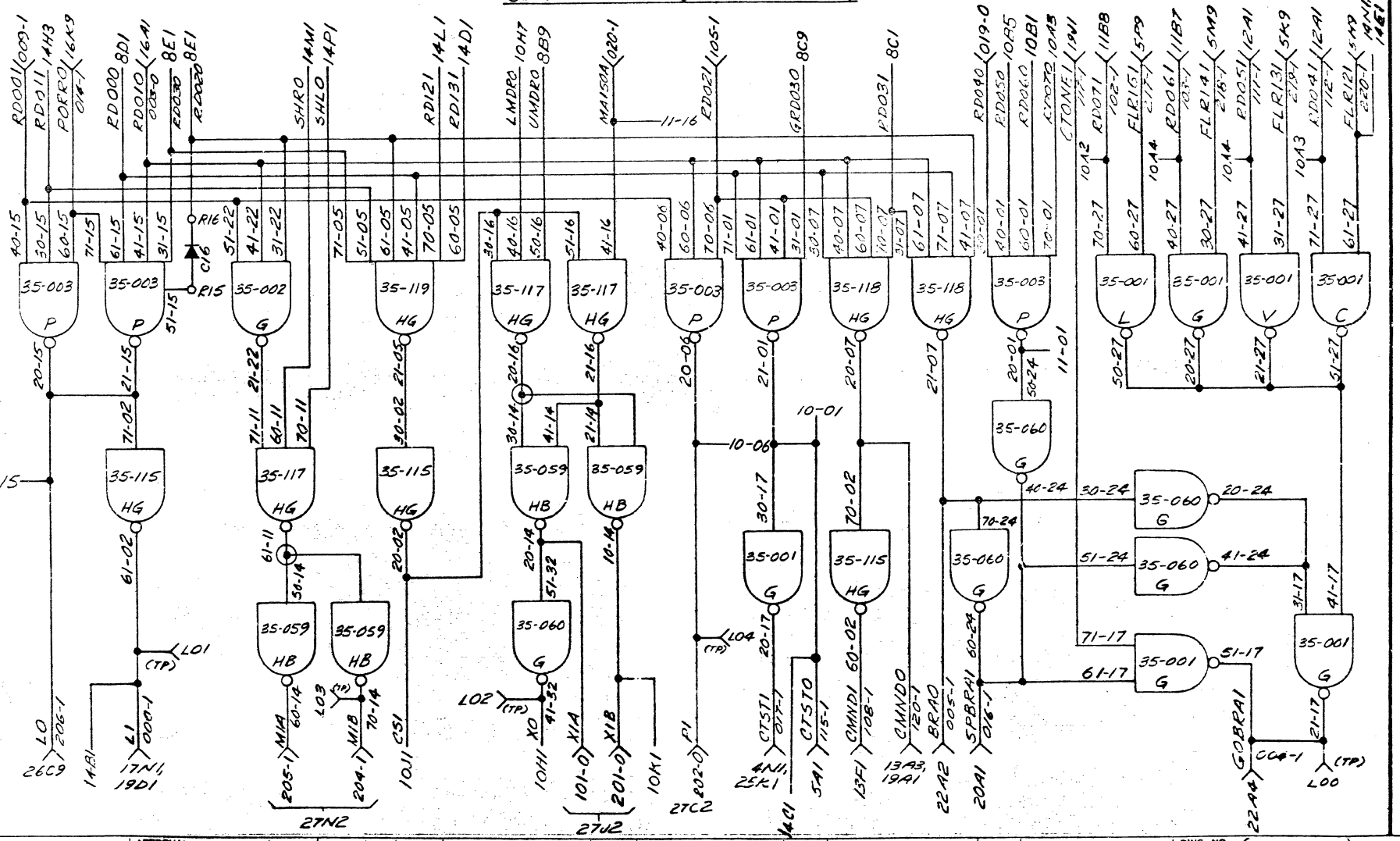
GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

DWG NO (FS 45)
70B1130008
CONT. ON SHEET 16 SH NO 15

CONTROL (ALU & BRANCH)

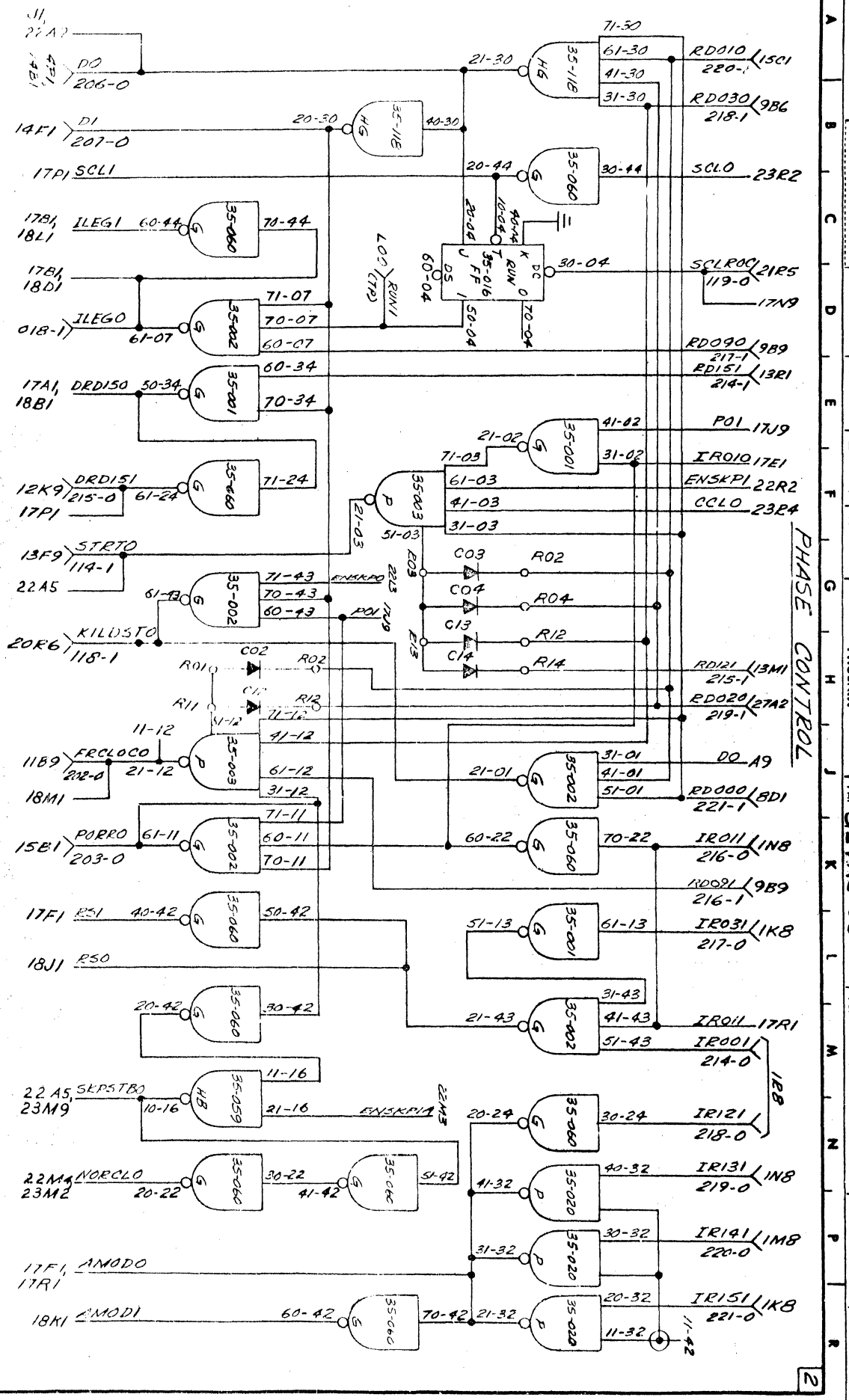
NOTE: 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON CONTROL O BD (COΦ).



MADE BY J. Katajisto JUNE 24, 69
ISSUED JUL 18 1969
APPROVAL E. A. White June 25, 69
DES.
CHKR. DP
REV. E

DWG. NO. (FS 45)
70B1130008
CONT ON SHEET 16 SH NO. 15

NOTES: 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON CONTROL 1 BD(C01).



DIST.

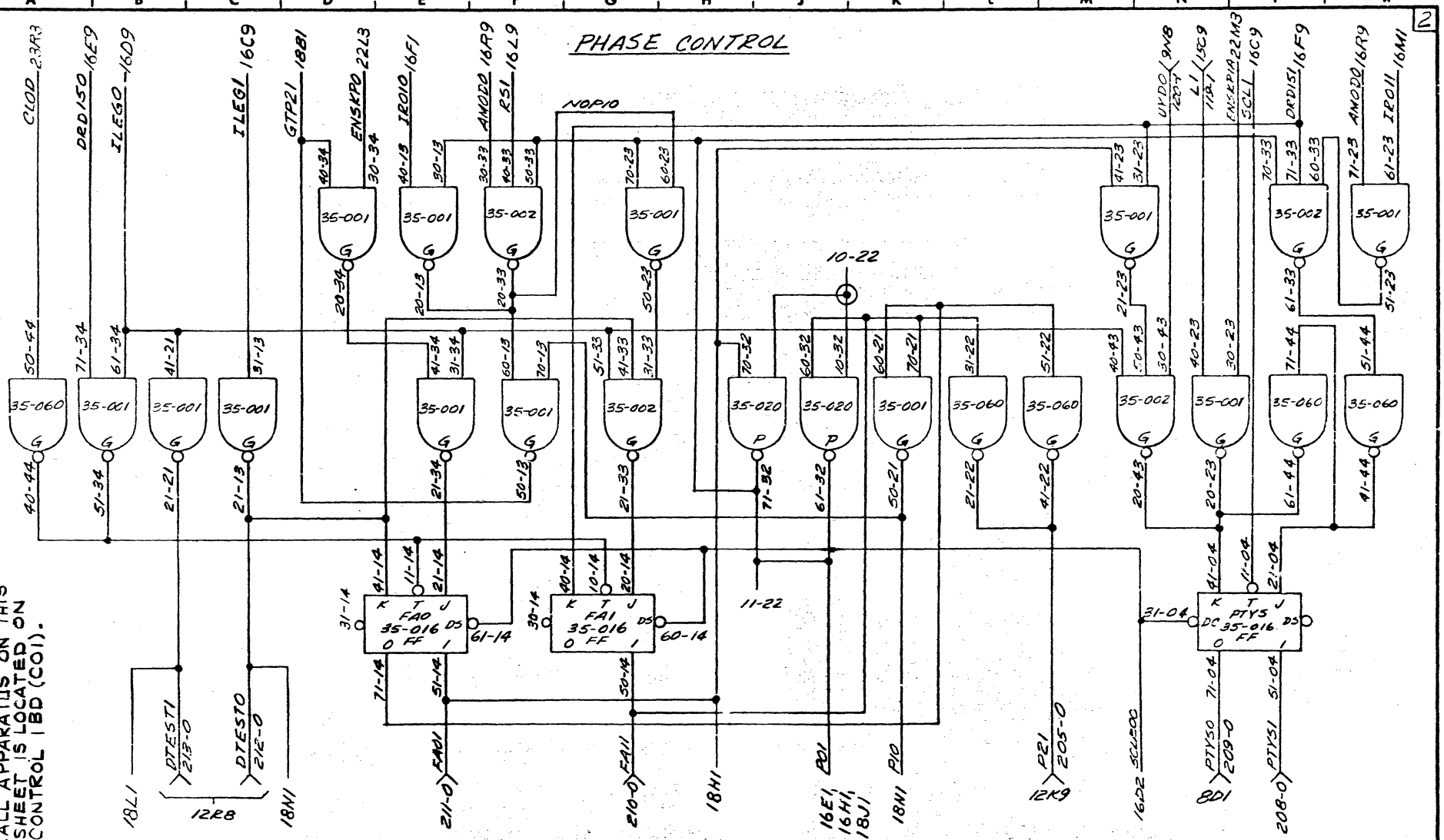
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:--
APPLIED PRACTICES | SURFACES ✓ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC, PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

DWG NO (FS45) 70B113008
CONT. ON SHEET 18 SH. NO 17

PHASE CONTROL



NOTES:
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON CONTROL 1BD (C01).

MADE BY J. Katajisto JUNE 24, 69
ISSUED JUL 18 1969
APPROVAL E. G. White June 25, 69
DES. | CHKR. DE | REV. E

DWG. NO. (FS45) 70B113008
CONT ON SHEET 18 SH NO. 17

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS		
		FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC,
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

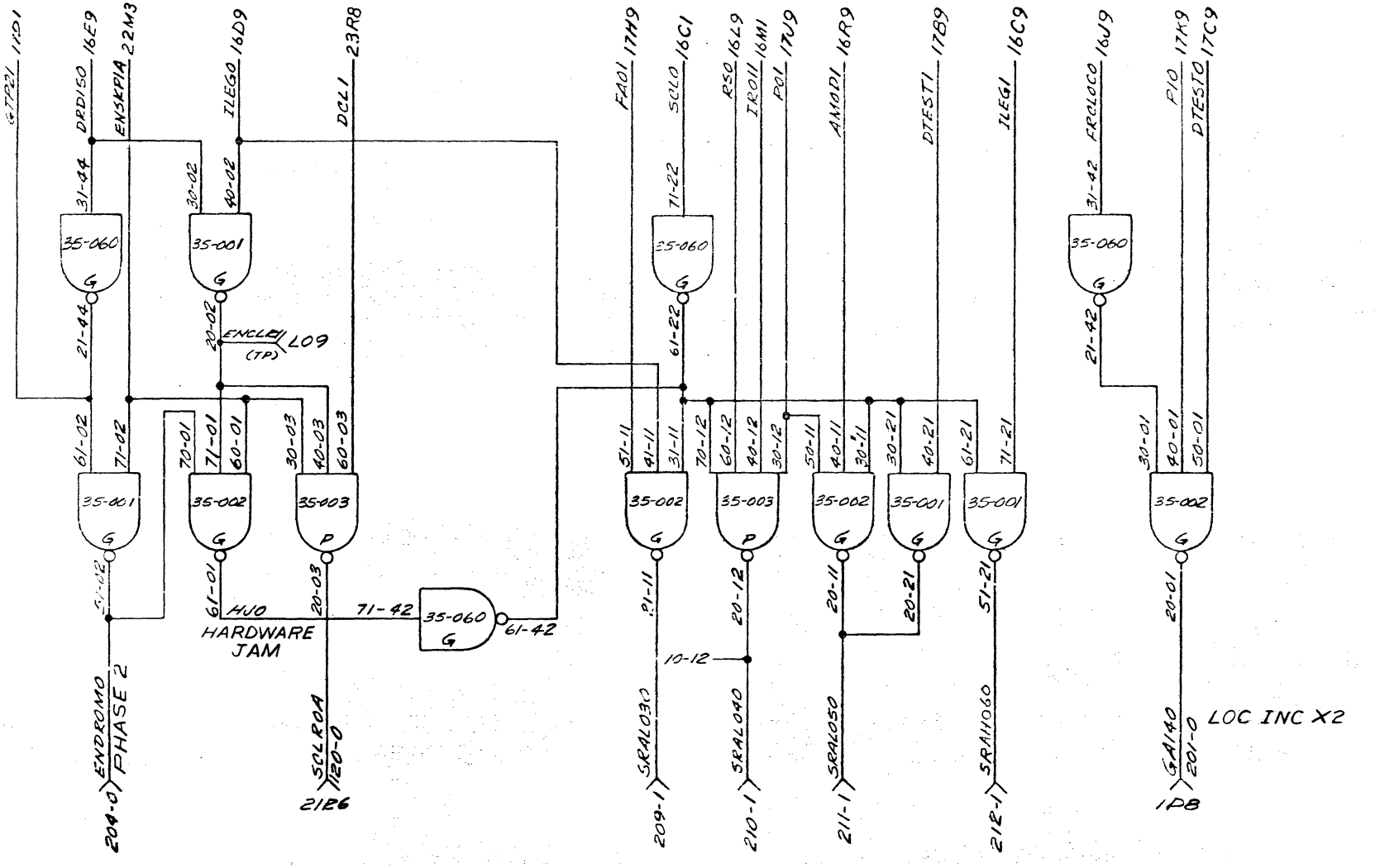
DWG. NO. (FS4S) 70B113008
CONT. ON SHEET 19 SH. NO. 18

A B C D E F G H J K L M N P R

PHASE CONTROL

2

NOTES:
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON CONTROL I BD(C01).



MADE BY J. Ratajiesk JUNE 24, 69
APPROVAL E. a. white June 25, 69
ISSUED JUL 18 1969

DES.
CHKR. DR
REV. E

DWG. NO. (FS4S) 70B113008
CONT ON SHEET 19 SH NO. 18

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC,
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

DWG NO (FS45) 70B113008
CONT. ON SHEET 20 SH NO 19

MODE CONTROL

NOTE:
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON THE CONTROL 2 BD.

MADE BY J. Katajinek JUNE 24, '69
ISSUED JUL 18 1969
DES. E. G. White June 25, 69
CHKR. DR
REV. E

DWG. NO. (FS45) 70B113008
CONT ON SHEET 20 SH NO. 19

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:--
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC.
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

DWG. NO. (FS45) 70B113008
CONT. ON SHEET 21 SH. NO. 20

MODE CONTROL

4

15L9 SPBRA1 / 016-1

19C9 FNYI0 — 35-060 G — MPY1

19A9 FNYI01 — 35-060 G — 35-060 G — L13 (TP)

SBD1 RPTI / 206-1

19D1 / 19L1 — (TP) L11

19B9 FNYI1 — 35-060 G

19M1 DVDI

19B9 FNYI00 — 35-060 G — 35-060 G — L12 (TP)

7L9 CEMTI

4C1 CSVI

5A9 FLR120

19L1 LI

19K1 IMPDVI

35-001 G — 35-115 HG

35-020 P — 35-002 G — 35-001 G — 35-003 P — 35-116 HG

FRCTPI1

DUDO

MPYO

19M9 FYDPI0 / 19N1 LO

CSVO

A1

19L9 FYDPI1 / 5A8 MPYI / 19M1

7M9 CEMTO

6P9 B150

DECTRO (216-0, 7A6)

DECTRI 19K1

19K2 — RDC41 — GRDO40 209-1 (11B7) — 11-37

LOB (TP) — ENDEST1 119-0 (10A2)

KILDSTO 220-0 (16M9)

L15 (TP) — FRALO70 (016-0)

NOTE:
1-ALL APPARATUS ON THIS SHEET IS LOCATED ON THE CONTROL 2 BD.

MADE BY J. Katajisto, JUNE 24, 69
ISSUED JUL 18 1969

APPROVAL E.G. White, June 25, 69

DES. | CHKR. DR

REV. E

DWG. NO. (FS45) 70B113008
CONT ON SHEET 21 SH. NO. 20

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±
SURFACES: √

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC,
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

DWG. NO. (FS45) 70B113008
CONT. ON SHEET 22 SH. NO. 21

INITIALIZE CONTROL (SEE NOTE 2)

NOTES:
1-ALL APPARATUS ON THIS SHEET IS LOCATED ON THE CONTROL 3 BD.
2, 35-082, 35-063 & 35-020 IN POS. 32 MAKE UP POWER FAIL DETECTION, SUPPLY ONLY UPON REQUEST.
3-CLIP TP LOT TO TPL08 TO INITIALIZE SYSTEM WITHOUT FIRMWARE SUPPORT.

12 VAC
S2 POWER
S2 INIT
35-063 PWR FAIL DETECTOR (NOTE 2)
NOTE 2 35-082
35-054 RELAY DRIVER
K30
POWER
P451 1K
PIFO
PIS +15V
POWDNO
SCLR0B
SCLR0C
SCLR0A
SCLR1
VPO
35-020 P
35-001 G
35-003 P
35-060 G
35-054 RELAY DRIVER

MADE BY J. Katajisk, JUNE 24, '69
ISSUED JUL 18 1969
APPROVAL E. A. White June 25, 69
DES. CHKR. DR REV. E

DWG. NO. (FS45) 70B113008
CONT ON SHEET 22 SH NO. 21

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

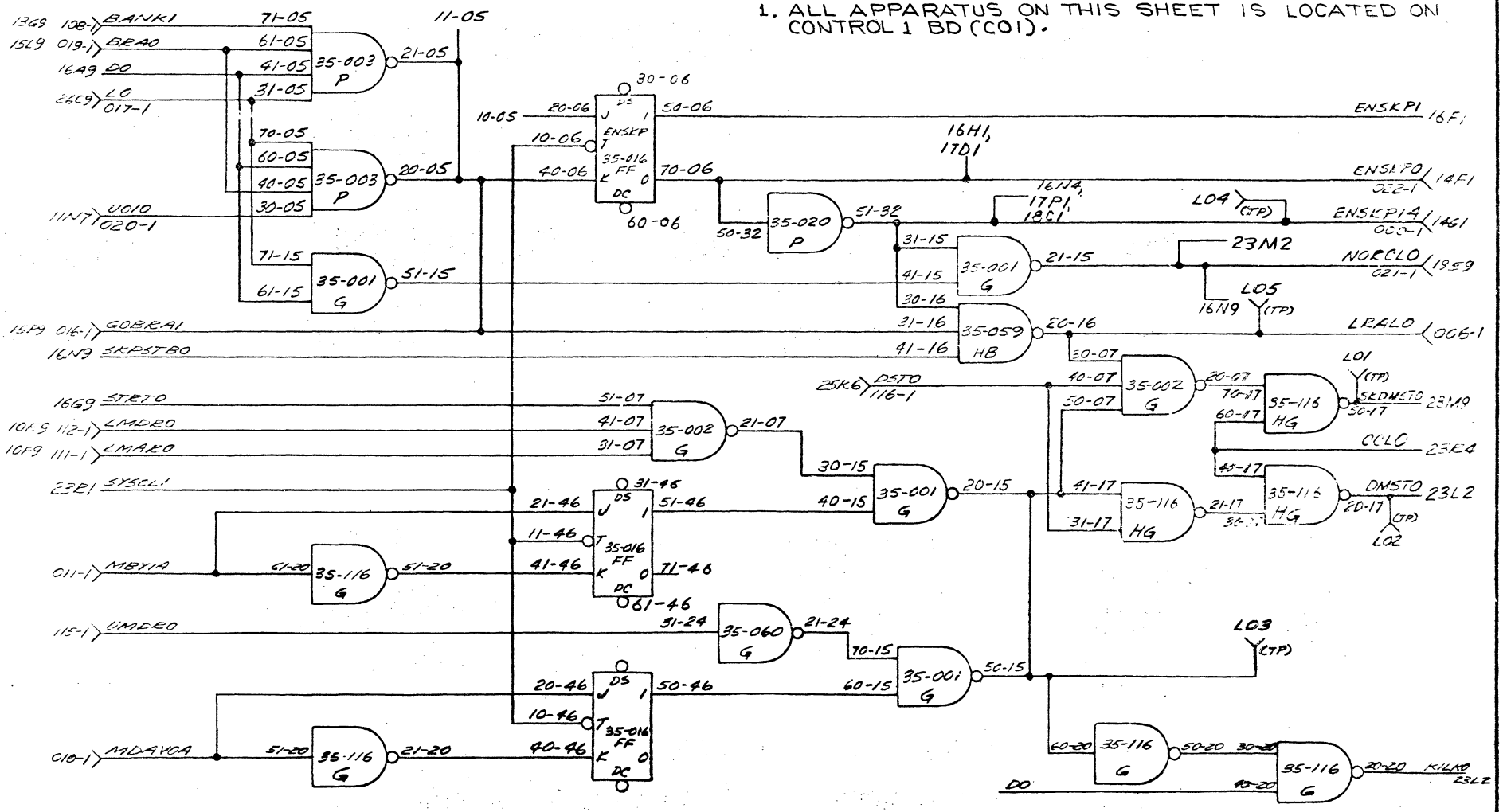
DWG NO (FS45) 70B113008
CONT. ON SHEET 23 SH NO 22

A B C D E F G H J K L M N P R

2

CLOCK CONTROL

NOTES:
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON CONTROL 1 BD (C01).



MADE BY L. Ratajack JUNE 24, 69
ISSUED JUL 18 1969

APPROVAL E. A. White June 25, 69
DES.
CHKR. DR
REV. E

DWG. NO. 70B113008
CONT ON SHEET 23 SH NO. 22

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES: V | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

DWG. NO. (FS45) 70B113008
CONT. ON SHEET 24 SH. NO. 23

CLOCK GENERATORS

NOTES:
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON CONTROL 1 BD (CO1).

MADE BY R. Katajisto JUNE 24, 69
APPROVAL E.G. White June 25, 69
DES.
CHKR. DR
REV. E
ISSUED JUL 18 1969

DWG. NO. (FS45) 70B113008
CONT ON SHEET 24 SH. NO. 23

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:--
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
PROCESSOR (MOD 30-2)
FMP GE-PAC 30 | FCF

DWG. NO. (FS45) 70B113008
CONT. ON SHEET 25 SH NO. 24

A B C D E F G H J K L M N P R

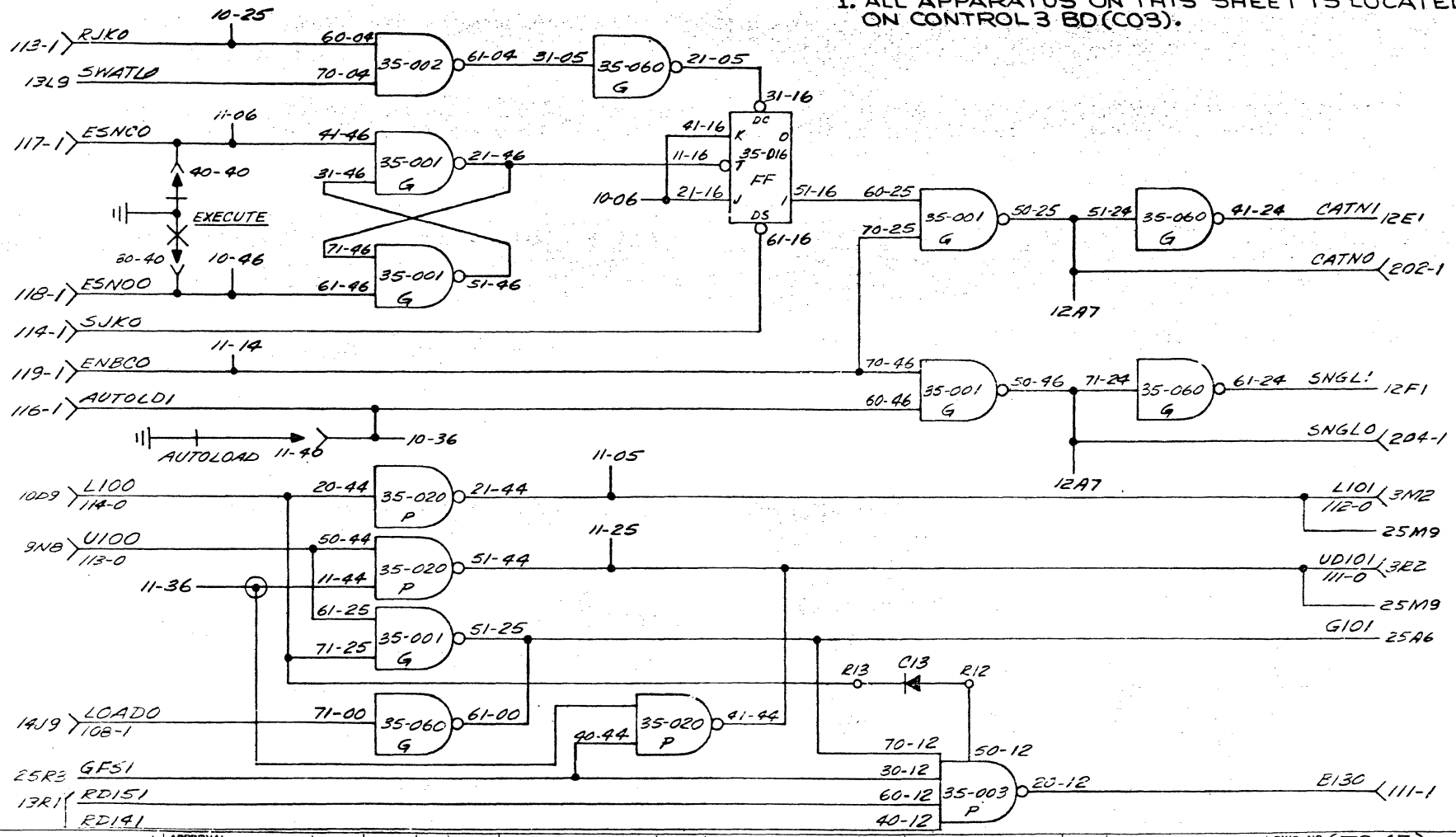
1 2 3 4 5 6 7 8 9

2

TOP SECTION
ONLY USED MODEL 30-1 WITHOUT DISPLAY

I/O CONTROL

NOTES:
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON CONTROL 3 BD (C03).



MADE BY	APPROVAL	DES.	REV.	DWG. NO (FS45) 70B113008
Kataja, JUNE 24, 69	E.G. White June 25, 69	CHKR. DR	E	CONT ON SHEET 25 SH NO. 24
ISSUED JUL 18 1969				

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES: V | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

DWG. NO. (FS45)
70B113008
CONT. ON SHEET 26 SH. NO. 25

A | B | C | D | E | F | G | H | J | K | L | M | N | P | R

2

I/O CONTROL

NOTES:
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON CONTROL 3 BD (C03).
2. FASTO (220-0) NORMALLY OPEN.

P5 47K 470PF 470PF 35-054
C25 1K R25 R24 C24 470PF R23
71-31 40-31 31-15 41-15 61-15 71-15 51-15
21-15 N.C. 11-15 B 35-027 G
FSYN1
RD121 13M1 CTST 1 15J9 203-1
11-11 (NOTE 2) 220-0 FASTO 30-17 35-002 G 20-17 20-16
11-25 30-25 35-001 G 20-25 34-36 95-001 G 20-36 40-16
J 1 35-016 T FF K 0 60-16 10-16
50-16 FST1 12R6
70-16 FST0 N.C.
50-16 SCLR0C 13L1
GFS1 24B9
SYN1 21E9
10-03 SYN0 120-1 31-00 35-060 G 21-00
30-06 40-06 50-06 35-117 HG 20-06
51-06 41-06 35-117 HG 21-06
51-23 35-060 G 41-23 L15 (TP)
60-06 70-06 35-117 HG 61-06
R36 C35 470PF R35
61-36 71-36 35-001 G 51-36 SV0 12:1-1 SK9
SCLIA 12H9
CCL1 13D1 51-05 35-060 G 41-05
30-07 40-07 50-07 35-117 HG 20-07
G101 24R7
SCL0 23R2 115-1 20-15 35-027 B 30-15
31-26 35-001 G 21-36
31-25 35-001 G 21-25
R16 C16 R15 R02 C02 100PF R01
81-26 41-26 11-26 21-26 DC K 0 35-016 T FF J 1 DS 71-26 51-26 DST0 22J5 110-1
D3 20-26 10-26 40-26 J 1 35-016 T FF K 0 DC 50-26 70-26 30-26 SOPC1
60-07 35-117 HG 61-07 SOPC1A
SCLR0C 13L1
L14 (TP)
N.C. 41-35 41-34 51-35 51-34 31-35 31-34 21-35 21-34
000 001 010 011 100 101 110 111
35-067 1 OF 8 DECODER
01 00 11 10 21 20 21 20
60-36 N.C. 60-34 DR0 116-0 70-35 ACK000 117-0 70-34 JR0 118-0 10-35 N.C. 10-34 DA0 119-0 20-35 ADRS0 120-0 20-34 CMD0 121-0
11-35 61-34 40-35 11-34 71-34 71-35 30-34 30-35
RD151 13R1 31-07 35-117 HG 21-07 ED150
24R6 U101 24R7 U0101
13R1 RD141 209-1 RD140

MADE BY R. Katajisto JUNE 24, 69
APPROVAL E. G. White June 25, 69
DES. CHK DR REV. E
ISSUED JUL 14 1969

DWG. NO. (FS45)
70B113008
CONT ON SHEET 26 SH NO. 25

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ±, DECIMALS ±, ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

DWG NO (FS45) 70B113008
CONT. ON SHEET 27 SH NO 26

ARITHMETIC CARRY CKT

2

NOTES:
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON BIT SLICE BOARDS 0, 1, 2 & 3.
2. ACSLI ON BS3.

BIT SLICE			
0	1	2	3
00	04	08	12
00	04	08	12
00	04	08	12
00	04	08	12
01	05	09	13
01	05	09	13
01	05	09	13
01	05	09	13
02	06	10	14
02	06	10	14
02	06	10	14
02	06	10	14
03	07	11	15
03	07	11	15
03	07	11	15
03	07	11	15
03	07	11	WTR

1P2 B--0
27B8 AK--0
27E2, 27L2, 28D2, 28L2 L1
27B8 AK--1 → 41L 19-016 HG pin 04
27R4 B--1 → 41L 19-016 HG pin 05 → pin 06
27H2, 28H2 B--1 → 41L 19-016 HG pin 12
27J8 AK--1 → 41L 19-016 HG pin 13 → pin 11
1N8 B--0
27J8 AK--0
28E2, 27P2 B--1
28B8 AK--1
1L8 B--0 → 41L 19-016 HG pin 09
28C8 AK--0 → 41L 19-016 HG pin 10 → pin 08
28J8 AK--0 → 41L 19-016 HG pin 02
1J8 B--0 → 41L 19-016 HG pin 01 → pin 03
28H2 B--1
28H8 AK--1
28L2 C--1
1589, 19N1, 22A2 LO / 006-1 → 45R 19-012 HB pin 05 → pin 06

42R 19-002 G: pins 04, 03, 05 → pin 06
43R 19-005 P: pins 01, 02, 04, 05 → pin 06
43R 19-005 P: pins 10, 13, 12, 09 → pin 08
42R 19-002 G: pins 13, 01, 02 → pin 12
42R 19-002 G: pins 10, 11, 09 → pin 08
42L 19-002 G: pins 04, 03, 05 → pin 06
43L 19-005 P: pins 01, 02, 04, 05 → pin 06
43L 19-005 P: pins 10, 12, 13, 09 → pin 08
42L 19-002 G: pins 13, 02, 01 → pin 12
42L 19-002 G: pins 10, 11, 09 → pin 08

C--1 / 008-1 → 4C1
C--1 / 000-0 → 4E1
27D2
C--0 → 27N2
44R 19-003 G: pins 02, 01 → pin 03 → LC--1 → 27L2
44R 19-003 G: pins 05, 04 → pin 06 → LC--1 → 28D2
C--0 → 28F2

BIT SLICE			
0	1	2	3
SV	03	07	11
00	04	08	12
01	05	09	13
01	05	09	13
02	06	10	14
02	06	10	14

MADE BY J. Ratajczak, JUNE 24, 69
ISSUED JUL 18 1969
APPROVAL E. A. White June 25, 69
DES.
CHKR. DR
REV. E

DWG NO (FS45) 70B113008
CONT ON SHEET 27 SH NO. 26

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

DWG. NO. (FS45) 70B113008
CONT. ON SHEET 28 SH. NO. 27

ARITHMETIC LOGIC UNIT

2

NOTES: 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON BIT SLICE BOARDS 0, 1, 2, & 3.

2. 212-0, BSO, WIRED TO GATED CARRY INPUT TRUE FOR SHIFT RIGHT (CTSRD).

MADE BY R. Katajisto JUNE 24, 69
ISSUED JUL 18 1969

APPROVAL E. A. White June 25, 69

DES. | CHKR. DR | REV. E

DWG. NO. (FS45) 70B113008
CONT ON SHEET 28 SH. NO. 27

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

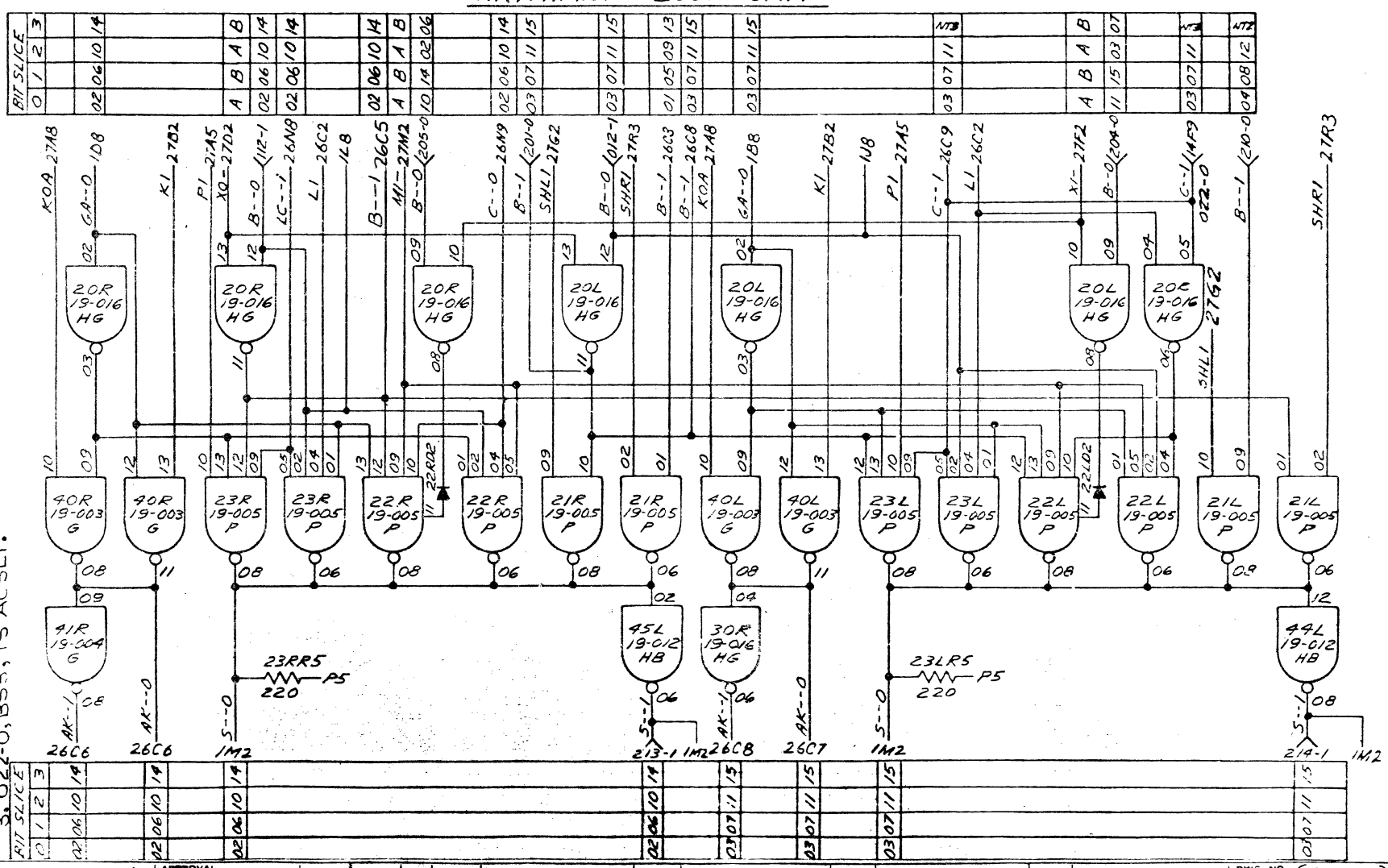
TITLE FUNCTIONAL SCHEMATIC
PROCESSOR (MOD30-2)
FMF GE-PAC 30 | FCF

DWG NO. (FS45) 70B113008
CONT. ON SHEET 29 SH. NO. 28

ARITHMETIC LOGIC UNIT

2

NOTES:
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON BIT SLICE BOARD 0, 1, 2, & 3.
2. 210-0, BS3, WIRED TO GATED CARRY SHIFT LEFT, TRUE (CTSL1).
3. 022-0, BS3, IS ACSL1.



MADE BY	APPROVAL	DES.	REV.		DWG NO. (FS45)
J. Ratajack JUNE 24, '69	E. a. white June 25, 69	CHKR. DP	E		70B113008
ISSUED JUL 18 1969					CONT ON SHEET 29 SH NO. 28

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

DWG NO (FS45) 70B113008
CONT. ON SHEET 30 SH NO 29

BACK PANEL MAP

		CONN POS	11			13				15			16		
		MOTH. BD	C00			C01				BS0			BS1		
		VERT. POS	HORIZ POS			HORIZ POS			HORIZ POS				HORIZ POS		
			0	1	2	0	1	2	0	1	2	0	1	2	0	1	2
		22	UIR40	P5	GND	ENSKP0	P5	GND				UIRO	P5	GND	UIR40	P5	GND
7		21	CEMT1	RPT1	U100	NDRCL0	STCLK0	RD000				WMAR1	RMAR1	AR031	NPSW1	RPSW1	AR071
		20	MA150A	CMND0	FLR121	U010	UY00	RD010				WMR11	RMR11	AR021	NMR31	RMR31	AR061
		19			FLR131	BRA0	L1	RD020				WMR41	RMR41	AR011	WMAR1	RMAR1	AR051
		18		L.SWO	FLR141	ILEG0	KILDSTO	RDD30				WMR01	RMR01	AR001	WMR11	RMR11	AR041
		17	CTST1	CTONE1	FLR151	L0		RD090				WLOC1	RLOC1	UD101	WMR41	RMR41	UD101
		16	SPBRA1	D1	D0	GOBRA1	DSTO	RD091				WMR21	RMR21	B080	WMR01	RMR01	B100
3		15	SCL0	CTSTO	LDF0	SCL0	UMDRO	RD121				WPSW1	RPSW1	B090	WLOC1	RLOC1	B110
		14	PORRO	PTYS1	PTYS0	POWO	STRTO	RD151				WMR31	RMR31	S031	WMR21	RMR21	S071
		13	RD030	RD031	LCTRO	PPF0	ATN0					B010	B000	S021	B050	B040	S061
		12	GRD040	RD041	L100	CCL0	LMDRO	SRAHC60				B030	B020	S011	B070	B060	S051
	1	11	RD050	RD051	ENSKP1A	MBYIA	LMARO	SRAL050				RD080	RD110	S001	RD080	RD100	S041
		10	ENSKP0	IR111	IR151	MDAV0A	CLKOFF0	SRAL040				RD100	RD030	IR031	RD111	RD030	IR071
4		09	RD001	IR101	IR141	ROMSTB0	EXTCLK0	SRAL030				DAL010	S091	IR021	DAL030	S111	IR061
		08	LIRO	IR091	IR131		BANK1					CSV1	LIRO	IR011	C031	LIRO	IR051
		07	SEVN1	IR081	IR121	STPSYS1						SEVN1	MIA	IR001	SEVN1	MIB	IR041
		06	RD011	LARO	L0	LRAL0	SCLR0					L0	S081	LARO	L0	S101	LARO
		05	BRA0	RD021	MIA	CD0	HLFCLK1					L101	DAL000	RD110	L101	DAL020	RD110
		04	GOBRA1	UA1	MIB	AUTOLD1	RCL0						UA1	UYD0		UA1	UYD0
		03	RD060	RD061	LMARO	P5	OSC1					RD090	UIRO	S0031	RD090	UIRO	S0471
5		02	EDOTO	RD071	LCC0	GND	VP0					RD091	RD081		RD091	RD081	
		01	ENDEST	SVAC0	SVAC1	CL0D						CL0D	DRL010	RD090	CL0D	DRL030	RD090
		00	L1	P5	GND	ENSKP1A	P5	GND				DRL000	P5	GND	DRL020	P5	GND
		22		P5	END		P5	GND				C031	P5	GND	C071	P5	GND
		21	SHL1	SVSC0			CL0E	IR151				SHL1	RD070	GA020	SHL1	RD071	GA060
6		20	CLRC				SCLR0A	IR141				U000	GRD040	RD050	U010	GRD040	RD060
		19	RD040	BANK1	U020		SCLR0C	IR131				WG071	RG071	BANK0	WG111	RG111	BANK0
		18	LOAD0	UMDRO	ENG1			IR121				WG061	RG061	ENG1	WG101	RG101	ENG1
		17	LMDH0	DB01	DB00		DCL1	IR031				WG051	RG051	DB00	WG091	RG091	DB00
		16	LMDL0	DB11	DB10			IR011				WG041	RG041	DB10	WG081	RG081	DB11
		15	STF0	B120	DB20			DRD151				WG031	RG031	DB20	WG071	RG071	DB20
		14	STFL0	B130	LMDRO			IR001				WG021	RG021	RD020	WG061	RG061	RD020
7		13	ACS0	B140	SHR1			DTEST1				WG011	RG011	B001	WG051	RG051	B041
		12	ACSL1	B150	CTSR1			DTEST0				WG001	RG001	CTSR1	WG041	RG041	B031
	0	11		RD081	CTSL1			FA01				WG151	RG151	SHR1	WG031	RG031	SHR1
		10	FLG00					FA11				WG141	RG141	B041	WG021	RG021	B081
		09		RD101	SB20			PTYS0				WG131	RG131	SB20	WG011	RG011	SB20
		08	FD110	CMND1				PTYS1				WG121	RG121	RD050	WG001	RG001	RD050
8		07	FD120	RD121				D1				WG111	RG111	B080	WG151	RG151	B120
		06	FD130	FD131	SB11			D0				WG101	RG101	B090	WG141	RG141	B130
		05		RD141	SB01			P21				WG091	RG091	B100	WG131	RG131	B140
		04		FD151				ENDROM0				WG081	RG081	B110	WG121	RG121	B150
		03	RD010	SBC0	DEVN1			PORR0				SB00	FYDP10	RD111	SB00	FYDP10	RD101
		02	RLG20	SE.0	P1			ERCL0C0				STCLK0	DEVN1	SB10	STCLK0	DEVN1	SB11
9		01	RD000	X1A	X1B			SA140				X1A	P1	B031	X1B	P1	B071
		00		P5	GND		P5	END				C001	P5	GND	C041	P5	GND

MADE BY J. Ratajczak, JUNE 24, '69
ISSUED JUL 18 1969

APPROVAL E. A. White June 25, 69

DES
CHKR DR

REV. E

DWG NO (FS45) 70B113008
CONT ON SHEET 30 SH NO. 29

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING
APPLIED PRACTICES | SURFACES ✓ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

DWG NO (FS 45)
70B113008
CONT ON SHEET 31 SH NO 30

BACK PANEL MAP

CONN POS	17			18			19						21					
MOTH. BD	BS2			BS3			C02						C03					
VERT. POS	HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS		
	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2
22	U100	P5	GND	UYDO	P5	GND		P5	GND					P5	GND			
21	WLOC1	RLOC1	AR111	WMR41	RMR41	AR151	FLR120	FLR121	SFL120					SVO	RD041			
20	WMR21	RMR21	AR101	WMR01	RMR01	AR141	FLR130	FLR131	SFL130					SYNO	RD051			
19	RPSW	RPSW1	AR09	WLOC1	RLOC1	AR131	FLR140	FLR141	SFL140					ENBCO	RD061			
18	WMR31	RMR31	AR081	WMR21	RMR21	AR121	FLR150	FLR151	SFL150					ESNOO	RD071			
17	WMAR1	RMAR1	UI101	GND	GND	UDI01	CTST1	CTR121	CTONE1					ESNCO	RD081			
16	WMR11	RMR11	B120	WMR31	RMR31	B140	SPBRA1	CTR131						AUTOLD1	RD091			
15	WMR41	RMR41	B130	WMAR1	RMAR1	B150		CTSTO	LDFO					SCLO	RD101			
14	WMR01	RMR01	S111	WMR11	RMR11	S151	S121	LCTRO	S141					SJKO	RD111			
13	B090	B080	S101	B130	B120	S141	S131	CTR141	S151					RJKO	RD121			
12	B110	B100	SC91	B150	B140	S131		CTR151						CCLO	RD131			
11	RD050	RD101	SC81	RD080	RD110	S121	RD041	FNY01	SOOY					B130	RD141			
10	RD111	RD030	IR111	RD101	RD030	IR151	RD051	FNY11						DSTO	RD151			
09	DAL050	S131	IR101	DAL070	S151	IR141	RD070	NORCL1	GRD040					ROMSTBO	RD140			
08	C071	LIRO	IR091	C111	LIRO	IR131	CSV1	FYDP11	CSVO					LOADO	WRMIO			
07	SEVN1	MIA	IR081	SEVN1	MIB	IR121		UTI						TTEST2	ATNO			
06	LO	S121	LARO	LO	S141	LARO	LO	CEMT1	RPT1					SOII	ARST1			
05	L101	DAL040	RD110	L101	DAL060	RD110		PTYS1	S1251					LPSWO	MPFO			
04	UPSWO	UA1	UYDO		UA1	UYDO	UPSWO		SB111					TTEST1	SNGLO			
03	FLO91	UIRO	SB111	RD091	UIRO	S1251		FAIL	S0471					DTEST2	CTST1			
02	RDO91	RDO81		RD091	RDO81	FRCLOCO	LCCO	FA01	S0031					DTEST1	CATNO			
01	CLOD	DRL050	RD090	CLOD	DRL070	RD090	CLOD	SVACO	SVAC1					CLOD	PPF1			
00	DRL040	P5	GND	DRL060	P5	GND	L1	P5	GND					P5	GND			
22	C111	P5	GND	ACSL1	P5	GND		P5	GND					P5	GND			
21	SHL1	RDO71	GA100	SHL1	RDO70	GA140	SHL1	SVSCO						CMDO	GND			
20	U030	GRD040	RD061	U020	GRD040	RD061	CLRO	CMNDO	KILDSTO					ADRSO	FASTO			
19	WG151	RG151	GND	WG031	RG031	BANK0		ENBES1						DAO	GND			
18	WG141	RG141	ENG1	WG021	RG021	ENG1			NORCLO					SRO	GND			
17	WG131	RG131	DB01	WG011	RG011	DB01	TTEST1	TTEST2						ACKOOO	GND			
16	WG121	RG121	DB10	WG001	RG001	DB11	FRALO70	DCL1	DECTRO					DRO	NKU			
15	WG111	RG111	DB20	WG151	RG151	DB20	STFO	B120	B000					CLO70	STRTO			
14	WG101	RG101	RD020	WG141	RG141	RD020	STFLO	B130						LICO	BANK1			
13	WG091	RG091	B081	WG131	RG131	B121		B140	SHR1					UICO	BANK0			
12	WG081	RG081	B071	WG121	RG121	B111		B150						LIO1	PFFO			
11	WG071	RG071	SHR1	WG111	RG111	SHR1		U000						UDIO1	POWO			
10	WG061	RG061	B121	WG101	RG101	CTSL1		DO						UT1	CMND1			
09	WG051	RG051	SB20	WG091	RG091	SB20		LRAMO						P21	STPSYS1			
08	WG041	RG041	RD050	WG081	RG081	RD050								DRD151	DPFO			
07	WG031	RG031	B000	WG071	RG071	B040								CMNDO	VPO			
06	WG021	RG021	B010	WG061	RG061	B050								CLRO	SCLR0			
05	WG011	RG011	B020	WG051	RG051	B060	S1O							F2RDBO	SCLR1			
04	WG001	RG001	B030	WG041	RT041	B070								F2RDAO	SCLR0A			
03	SB01	FYDP10	RD100	SB01	FYDA10		FYDP10	SCLROC	DEVN1					F1RDBO	SCLR0B			
02	STCLK0	DEVN1	SB10	STCLK0	DEVN1	SB11								F1RDAO	SCLR0C			
01	X1A	P1	B111	X1B	P1	B151								P15	N15			
00	C081	P5	GND	C121	P5	GND	C001	P5	GND					P5	GND			

MADE BY J. Katajisto JUNE 24 69
ISSUED JUL 1 8 1969

APPROVAL E. A. White June 25, 69

DES.
CHKR. DR

REV. E

DWG NO (FS45)
70B113008
CONT ON SHEET 31 SH NO. 30

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
PROCESSOR (MOD 30-2)
FMF GE-PAC 30 | FCF

DWG NO (FS45) 70B113008
CONT ON SHEET F SH NO 3

S BUS (16 BITS, PARALLEL)

S (8:15) LIO
DAL (0:7)
CL (0:7) IO
8
I/O CONTROL
RD (14:15)
16
INPUT-OUTPUT DEVICE CONTROLLER
DRL (0:7)
INIT
SYNC
UIO
ATN
PSWOI
DISPLAY
CATN
SNGL

S (12:15) S (8:15)
4 RAH 7
4 RAS 7 | 0 RAL 7
READ ONLY MEMORY (ROM)
0 RD 15
OP | D | S | E

S (0:7) 16
0 MAR 15
CORE MEMORY
16
0 MDH 7 | 0 MDL 7
LMDH
LMDR
LMDL

S (8:15) S (0:15)
0 IR 15
OP | YD | YS
IR4
4

16
0 MR0 15
0 MR1 15
0 MR2 15
0 MR3 15
0 MR4 15
0 MAR 15
0 LOC 15
0 PSW 11
0 TR00 15
0 TR01 15
GENERAL REGISTERS
0 TR14 15
0 TR15 15

S (12:15) S02:15 16
FLR 12 15 C V G L
CTR 12 15
CCR 12 15

DECODER HARDWARE AND READ ONLY MEMORY (DROM)
IR (0:15)
16
PROCESSOR CONTROL
IMMEDIATE OR BRANCH

0 AR 15
ENABLE AR TO ALU
ARITHMETIC LOGIC UNIT (ALU)
CROSS SHIFT LOGIC

B (8:15) B (8:15) B(0:7) B (8:15) 16 B (12:15) 16 B(0:7) B(8:15) B (12:15)

B BUS (16 BITS PARALLEL)

MADE BY J. Katzaroff JUNE 24, 69
ISSUED JUL 18 1969
APPROVAL E. A. Nowlin June 25, 69
DES.
CHKR. DR
REV. E

DWG NO (FS45) 70B113008
CONT ON SHEET F SH NO 31

GENERAL ELECTRIC

PROCESS COMPUTERS
PHOENIX ARIZONA

TITLE FUNCTIONAL SCHEMATIC

4096-16 MEMORY BLOCK

DRAWING NUMBER	CONT.	PAGE
70B113009	0A	0

FIRST MADE FOR
GE-PAC 30
(FS50)

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
C	ISSUED				

REISSUED

C	Issued										

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME

REISSUED

(FS50)

MADE BY	APPROVAL	REV.											DWG. NO.	CONT.	PAGE
C. Ellsworth JUN.25;69	[illegible] E. G. White June 26,69	C											70B113009	0A	0
ISSUED July 18, 1969													PRINTS TO: K7-08		

PCE 2004

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30 | FCF

DWG NO (FS 50) 70B113009
CONT. ON SHEET 1 SH NO 0A

SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
SHEET INDEX SUPPORTING INFORMATION	0A	1	2																		
(BIT) B ACCESS	1	1	1																		
	2	1	1																		
	3	1	1																		
	4	1	1																		
ADDRESS BLOCK DECODER	5	1	1																		
B LOGIC	6	1	1																		
B CURRENT DRIVER	7	1	1																		
	8	1	1																		
	9	1	1																		
	10	1	1																		
	11	1	2																		
X ACCESS	12	1	1																		
	13	1	1																		
X LOGIC	14	1	2																		
X LINE DECODERS	15	1	1																		
X LINE SWITCHES	16	1	1																		
X LINE DECODERS	17	1	1																		
X LINE SWITCHES	18	1	1																		
X COLUMN DECODERS	19	1	1																		
X COLUMN SWITCHES	20	1	1																		
X COLUMN DECODERS	21	1	1																		
X COLUMN SWITCHES	22	1	1																		
READOUT	23	1	1																		
STROBE TIMING	24	1	1																		
ADDRESS BUFFER	25	1	1																		
	26	1	1																		
BACK PANEL MAP	27	1	1																		
	ISSUE DATE	6-10-69																			

SUPPORTING INFORMATION

CATEGORY	PART NO.
MOTHER BD (MEMORY	
CURRENT DRIVER (MCD)	32-009 F01 B01
	32-009 B02 B01
SWITCH (MSW) - K	32-010 B01
" -4K	32-010 F01 B01
ASSEMBLY (4K x 16 BIT)	32-011 B01 B01
" (4K x 18 BIT)	32-012 B01 B01
" (2K x 16 BIT)	32-013 B01 B01
" (2K x 18 BIT)	32-014 B01 B01

SHEET INDEX NOTES:

1. CHANGES ON THIS DRAWING SHALL REQUIRE ONLY THE REISSUE OF SHEETS AFFECTED.
2. THE ISSUE OF THIS SHEET SHALL DETERMINE THE LATEST ISSUE OF THIS DRAWING.

MADE BY E. Ellsworth JUN. 25, '69
ISSUED JUL 18 1969

APPROVAL E. G. White June 26, 69

DES.
CHKR. DR

REV. C

DWG. NO (FS 50) 70B113009
CONT ON SHEET 1 SH NO. 0A

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING				
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30 | FCF

DWG NO (FS50) 70B113009
CONT. ON SHEET 2 SH NO 1

(BIT) B ACCESS

TO B CURRENT DRIVERS

3RS 7RS 11R3

MEM "0" 35-028

MEM "1" 35-029

BW00 220-0 BW02 121-0 BW04 221-0 BW06 201-1 BW08 101-1 BW10 202-1 BW12 102-1 BW14 203-1 BW16 103-1

CORE PLANE BIT WIRES

BW0-0 BW0-1 BW0-2 BW0-3 BW0-4 BW0-5 BW0-6 BW0-7 BW2-0 BW2-7 BW4-0 BW4-7 BW14-0 BW14-7 BW16-0 BW16-7

BS10N BS10P BS11N BS11P BS12N BS12P BS13N BS13P BS14N BS14P BS15N BS15P BS16N BS16P BS17N BS17P

1K 1K 1K 1K

3RS

P15 N15

MADE BY	APPROVAL								
E. Ellsworth JUN.25,'69	E. A. White June 26, 69	DES	REV.	C					
ISSUED JUL 18 1969		CHKR.							

DWG NO (FS50) 70B113009
CONT ON SHEET 2 SH NO 1

DIST.

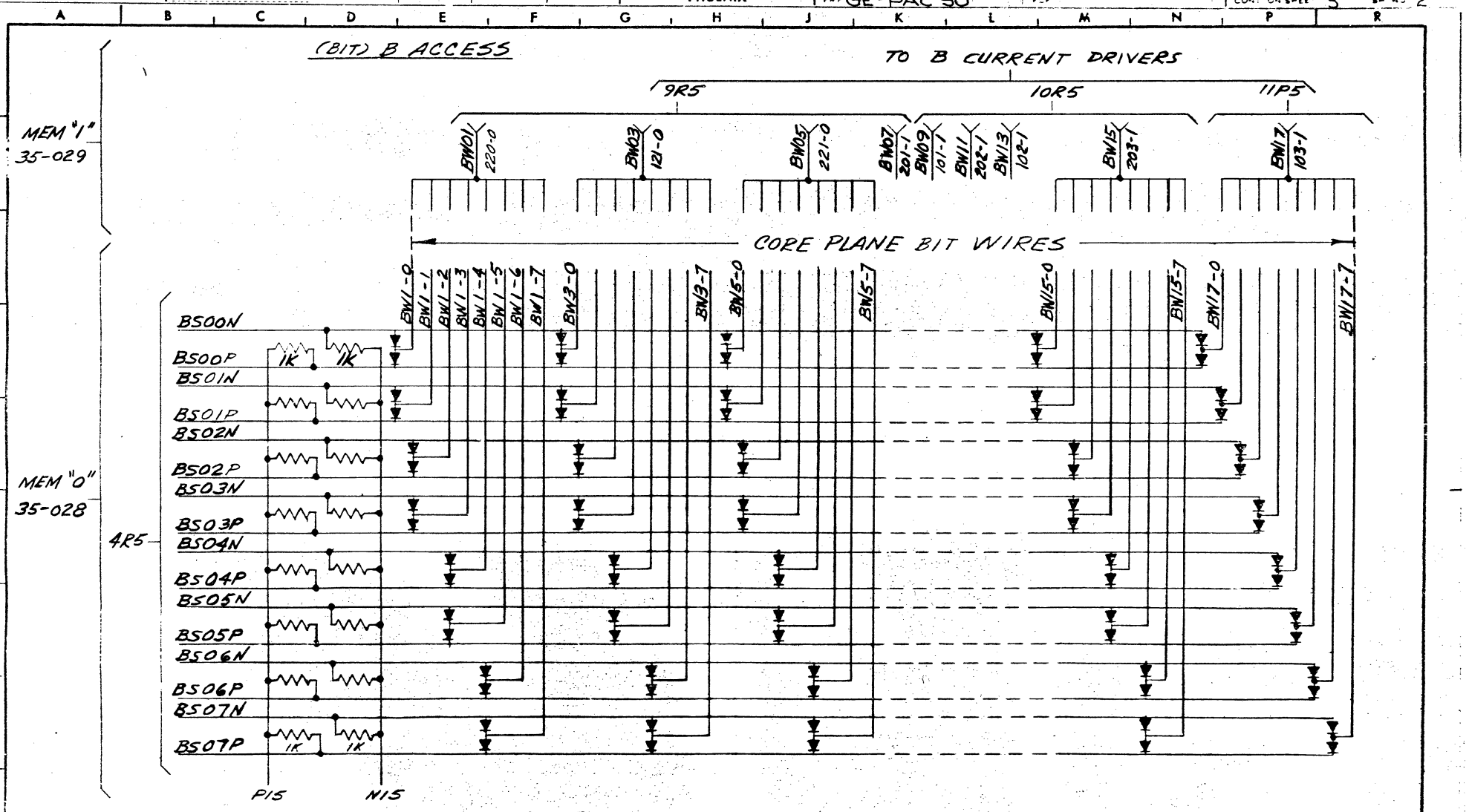
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS		
		FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30 FCF

DWG NO (FS50)
70B113009
CONT ON SHEET 3 SH NO 2



MADE BY
G. Ellsworth JUN. 25, '69
ISSUED JUL 18 1969

APPROVAL

DES.
CHKR. DR

REV. C

DWG NO (FS50)
70B113009
CONT ON SHEET 3 SH NO 2

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS		
		FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

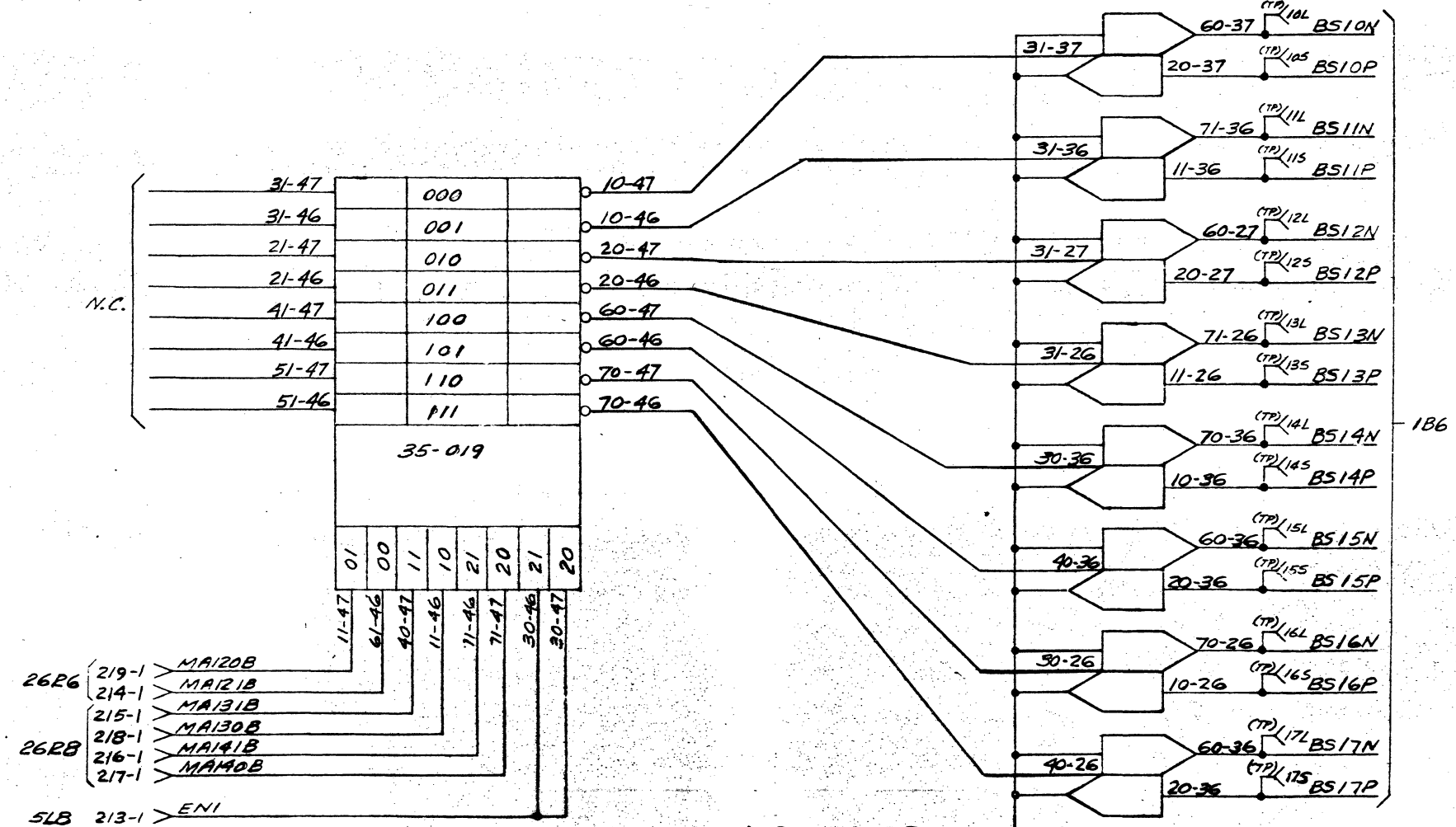
GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30 | FCF

DWG NO (FS50) 70B113009
CONT ON SHEET 4 SH NO 3

(BIT) B ACCESS

[ALL 35-006]



NOTES: 1. APPARATUS LOCATED ON MEMORY I BOARD (MEI). SWITCHES SELECT EVEN DATA BITS.

MADE BY G. Ellsworth JUN. 25, 69
ISSUED JUL 18 1969

CHKD. DR
REV. C

DWG NO (FS50) 70B113009
CONT ON SHEET 4 SH NO. 3

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30 | FCF

DWG NO (FS50) 70B113009
CONT ON SHEET 5 SH NO 4

(BIT) B ACCESS

[ALL 35-006]

N.C.

31-47	000	10-47
31-46	001	10-46
21-47	010	20-47
21-46	011	20-46
41-47	100	60-47
41-46	101	60-46
51-47	110	70-47
51-46	111	70-46

35-019

01 00 11 10 21 20 21 20

11-47 61-46 40-47 11-46 71-46 71-47 30-46 30-47

26P6 2J-1 > MA12DB
2J4-1 > MA12B
2J5-1 > MA13B
2J8-1 > MA13DB
26P8 2J6-1 > MA14B
2J7-1 > MA14DB
5L8 2J3-1 > ENI

31-37	60-37	(TP) 001L BS00N
	20-37	(TP) 005 BS00P
31-36	71-36	(TP) 011 BS01N
	11-36	(TP) 015 BS01P
31-27	60-27	(TP) 021 BS02N
	20-27	(TP) 025 BS02P
31-26	71-26	(TP) 031 BS03N
	11-26	(TP) 035 BS03P
30-36	70-36	(TP) 041 BS04N
	10-36	(TP) 045 BS04P
40-36	60-36	(TP) 051 BS05N
	20-36	(TP) 055 BS05P
30-26	70-26	(TP) 061 BS06N
	10-26	(TP) 065 BS06P
40-26	60-36	(TP) 071 BS07N
	20-36	(TP) 075 BS07P

286

NOTES:
1. APPARATUS LOCATED ON MEMORY 0 BOARD (ME0). SWITCHES, SELECT ODD DATA BITS.

MADE BY C. Ellsworth JUN.25,'69
ISSUED JUL 18 1969
APPROVED E.A. White June 26, 69
DES
CHKR DR
REV. C

DWG NO (FS50) 70B113009
CONT ON SHEET 5 SH NO 4

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30 | FCF

DWG. NO. (FS50)
70B113009
CONT. ON SHEET 6 SH. NO. 5

A B C D E F G H J K L M N P R

1FS28

MA000A (213-1)
MA010A (113-1)
MA020A (214-1)
MA030A (114-1)

P5

60-04 70-04 30-04 40-04 61-04 71-04 31-04 41-04

35-001 35-001 35-001 35-001

50-04 20-04 21-04 51-04

70-03 71-03 61-03 51-03 41-03 31-03 21-03 11-03

(01) (00) (11) (10) (21) (20) (31) (30)

ADDRESS BLOCK 35-038
(SEE TABLE A)

(C) (1) (2) (3)

60-03 50-03 30-03 10-03

21-02
31-02
41-02
51-02
11-02

35-022

60-02

5FS28 116-C) MEN1

R01

112-1 205-1

ENOA

R02
470
P5

35-022 P

70-02 EN1 212-1 (3A9 4A9)

R03

6B1

110-1 204-1

ENOB

14B1

ENABLE INTERLOCK ON MEMORY '0' BOARD

TABLE A: ADDRESS BLOCK DECODER

ADDRESS FIELD					ADDRESS BLOCK CONNECTION							
HEX	BINARY				FOR 4K BYTE BLOCKS:				FOR 8K BYTE BLOCKS:			
	0	1	2	3	60	50	30	10	60	50	30	10
0XXX	0	0	0	0	71	51	31	11	71	51	31	N.C.
1XXX*	0	0	0	1	71	51	31	21				
2XXX	0	0	1	0	71	51	41	11	71	51	41	N.C.
3XXX*	0	0	1	1	71	51	41	21				
4XXX	0	1	0	0	71	61	31	11	71	61	31	N.C.
5XXX*	0	1	0	1	71	61	31	21				
6XXX	0	1	1	0	71	61	41	11	71	61	41	N.C.
7XXX*	0	1	1	1	71	61	41	21				
8XXX	1	0	0	0	70	51	31	11	70	51	31	N.C.
9XXX*	1	0	0	1	70	51	31	21				
AXXX	1	0	1	0	70	51	41	11	70	51	41	N.C.
BXXX*	1	0	1	1	70	51	41	21				
CXXX	1	1	0	0	70	61	31	11	70	61	31	N.C.
DXXX*	1	1	0	1	70	61	31	21				
EXXX	1	1	1	0	70	61	41	11	70	61	41	N.C.
FXXX*	1	1	1	1	70	61	41	21				

(*) ODD NUMBERED 4K BYTE BLOCKS REQUIRE A JUMPER BOARD IN LOCATION 33 OF MSW WITH PIN 21 (MA031B) CONN TO GND.

NOTES:
1. UNLESS OTHERWISE SPECIFIED, APPARATUS LOCATED ON MEMORY CURRENT DRIVER BOARD, (MCD).

MADE BY C. Ellsworth JUN. 25, 69
ISSUED JUL 18 1969
APPROVAL E. A. White June 26, 69
DES.
CHKR. DR
REV. C

DWG. NO. (FS50)
70B113009
CONT ON SHEET 6 SH NO. 5

DIST.

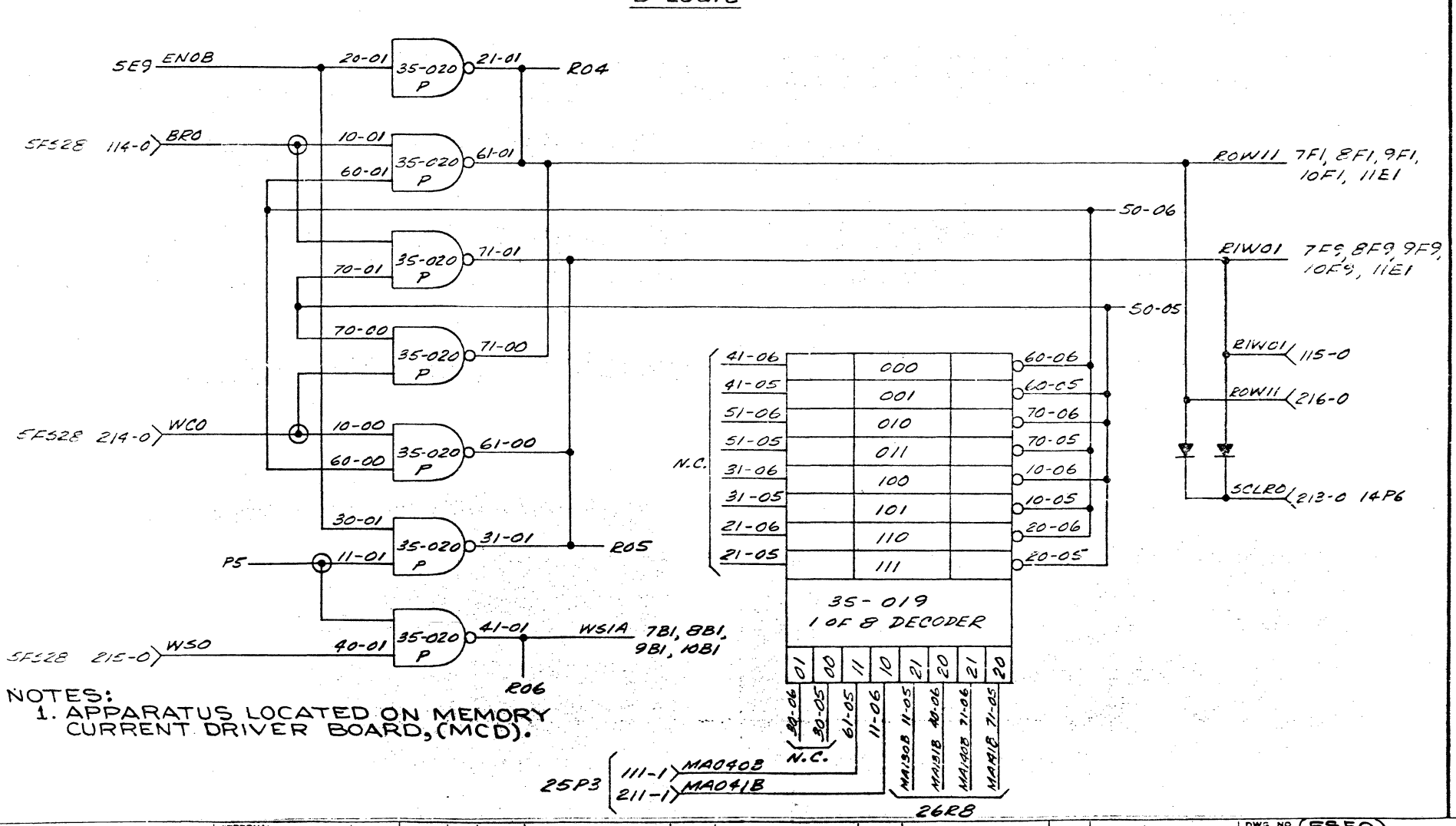
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30 | FCF

DWG. NO. (FS50) 70B113009
CONT. ON SHEET 7 SH. NO. 6

B LOGIC



NOTES:
1. APPARATUS LOCATED ON MEMORY CURRENT DRIVER BOARD, (MCD).

MADE BY E. Ellsworth JUN. 25, 69
ISSUED JUL 18 1969
APPROVAL E.A. White June 26, 69
DES.
CHKR DR
REV. C

DWG NO. (FS50) 70B113009
CONT ON SHEET 7 SH NO. 6

DIST.

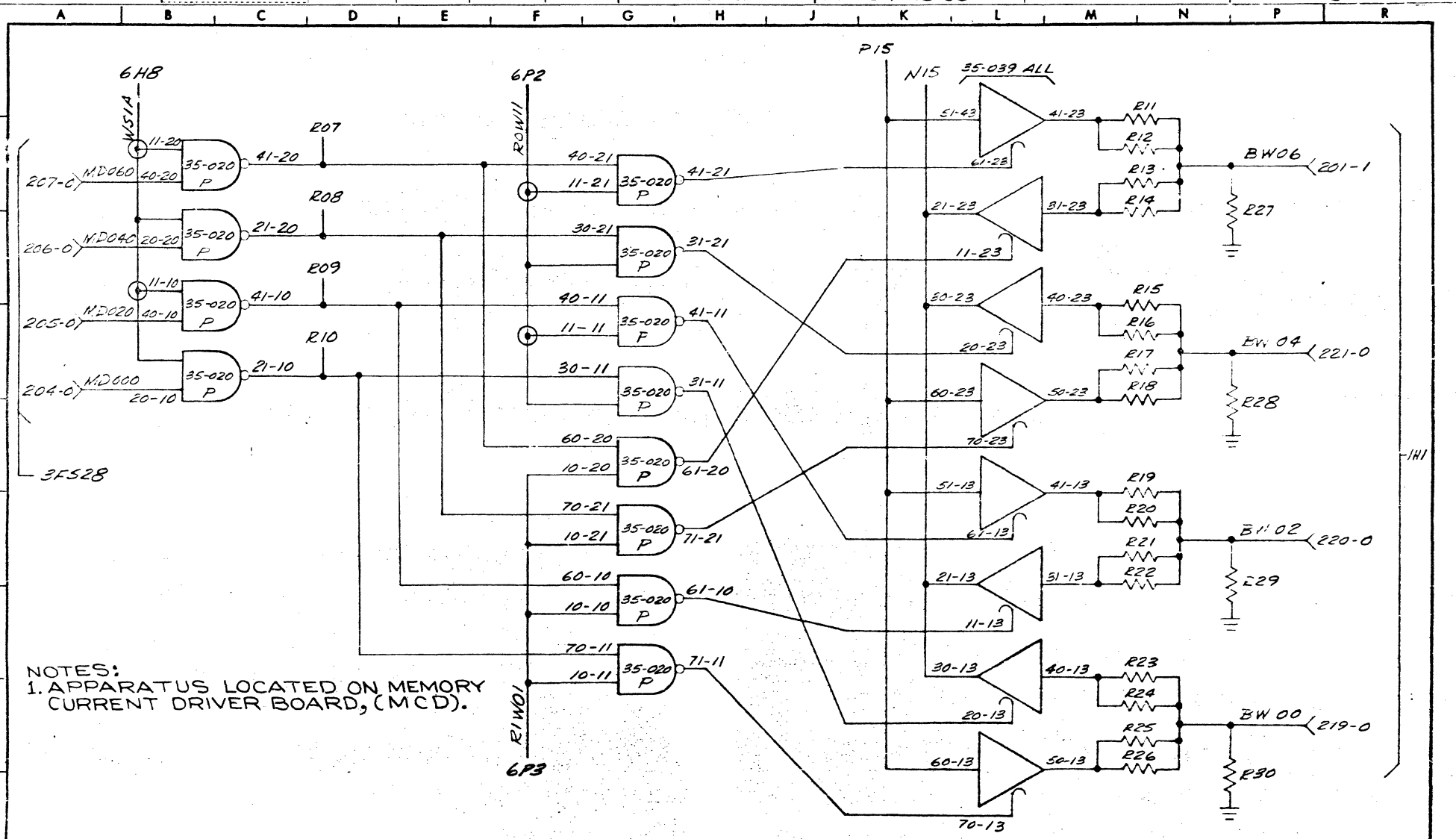
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30 | FCF

DWG NO (FS50) 70B113009
CONT ON SHEET 8 SH NO 7



NOTES:
1. APPARATUS LOCATED ON MEMORY CURRENT DRIVER BOARD, (MCD).

MADE BY E. Ellsworth JUN. 25, 69
ISSUED JUL 18 1969

APPROVAL E. G. White June 26, 69

DES.
CHKR DR

REV. C

DWG. NO (FS50) 70B113009
CONT ON SHEET A SH NO. 7

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

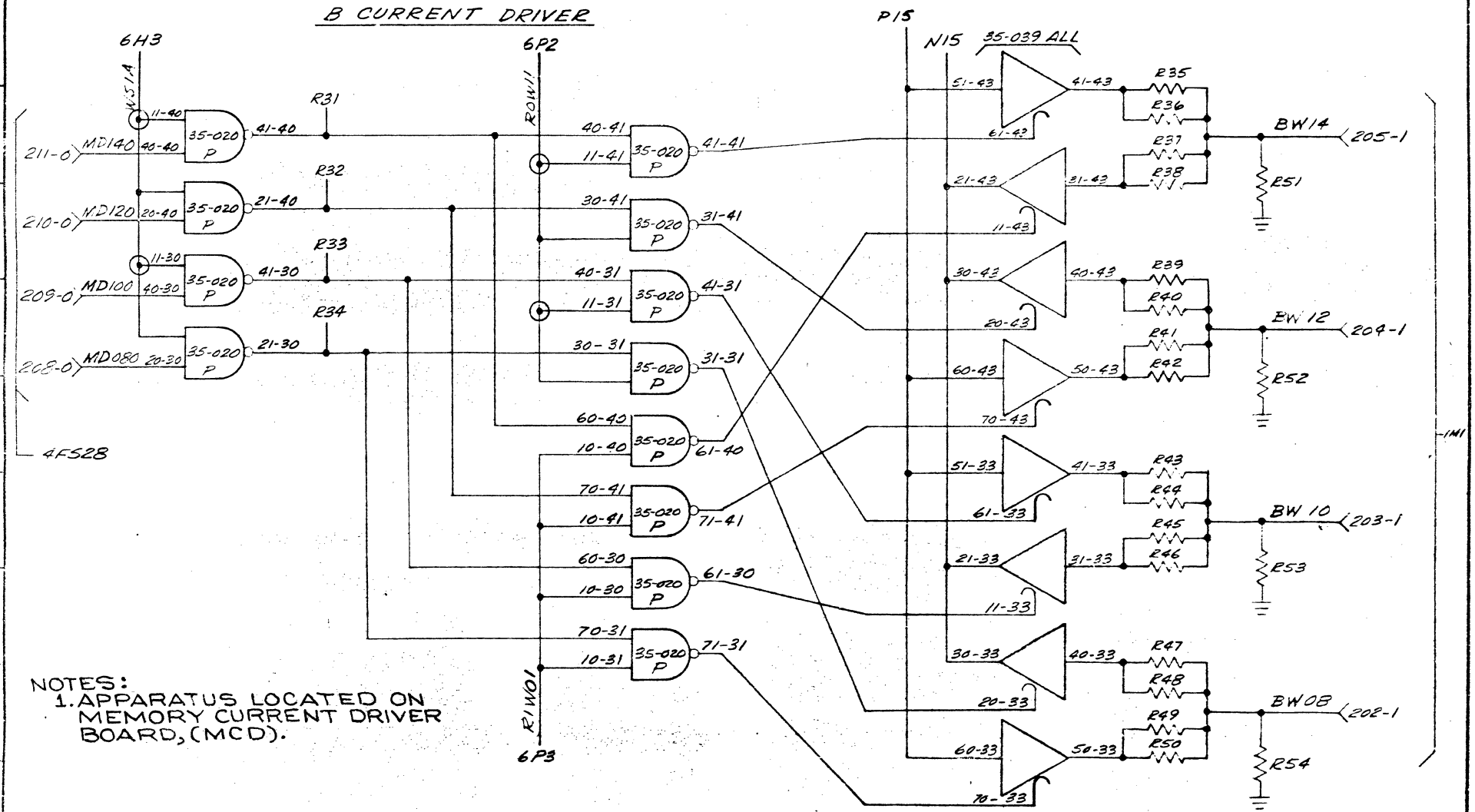
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS		
		FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30 | FCF

DWG NO (FS50)
70B113009
CONT ON SHEET 9 SH NO 8

B CURRENT DRIVER



NOTES:
1. APPARATUS LOCATED ON MEMORY CURRENT DRIVER BOARD, (MCD).

MADE BY C. Ellsworth JUN. 25, 69
ISSUED JUL 18 1969

APPROVAL E. A. White June 26, 69

DES.
CHKR. DR

REV. C

DWG NO (FS50)
70B113009
CONT ON SHEET 9 SH NO 8

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING —

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30 | FCF

DWG NO (FS50) 70B113009
CONT ON SHEET 10 SH NO 9

B CURRENT DRIVER

6A8 — W51A — 11-20 — 35-020 P — 51-20 — E55
10T-0 — MDO70 — 50-20
E56 — 31-20
E57 — 11-10 — 35-020 P — 51-10
10S-0 — MDO30 — 30-10
E58 — 31-10
10C-0 — MDO00 — 30-10
3FS28

6P2 — ROW11
50-21 — 11-21 — 35-020 P — 51-21
20-21 — 35-020 P — 21-21
50-11 — 11-11 — 35-020 P — 51-11
20-11 — 35-020 P — 21-11
70-20 — 10-20 — 35-020 P — 71-20
60-21 — 10-21 — 35-020 P — 61-21
70-10 — 10-10 — 35-020 P — 71-10
60-11 — 10-11 — 35-020 P — 61-11
R1W01 — 6P3

P15 — N15 — 35-039 ALL

40-22 — 20-22 — 30-22 — R59 R60 — BW07 (101-1
50-22 — 70-22 — 60-22 — R61 R62 — R75
21-22 — 11-22 — 31-22 — R63 R64 — BW05 (121-0
51-22 — 61-22 — 41-22 — R65 R66 — R76
40-12 — 20-12 — 30-12 — R67 R68 — BW03 (120-0
50-12 — 70-12 — 60-12 — R69 R70 — R77
21-12 — 11-12 — 31-12 — R71 R72 — BW01 (119-0
51-12 — 61-12 — 41-12 — R73 R74 — R78

-2H1

NOTES:
1. APPARATUS LOCATED ON MEMORY CURRENT DRIVER BOARD, (MCD).

MADE BY E. Ellsworth JUN. 25, '69
ISSUED JUL 18 1969
APPROVAL E. A. White June 26, 69
DES.
CHKR. DR
REV. C

DWG NO (FS50) 70B113009
CONT ON SHEET 10 SH NO 9

DIST.

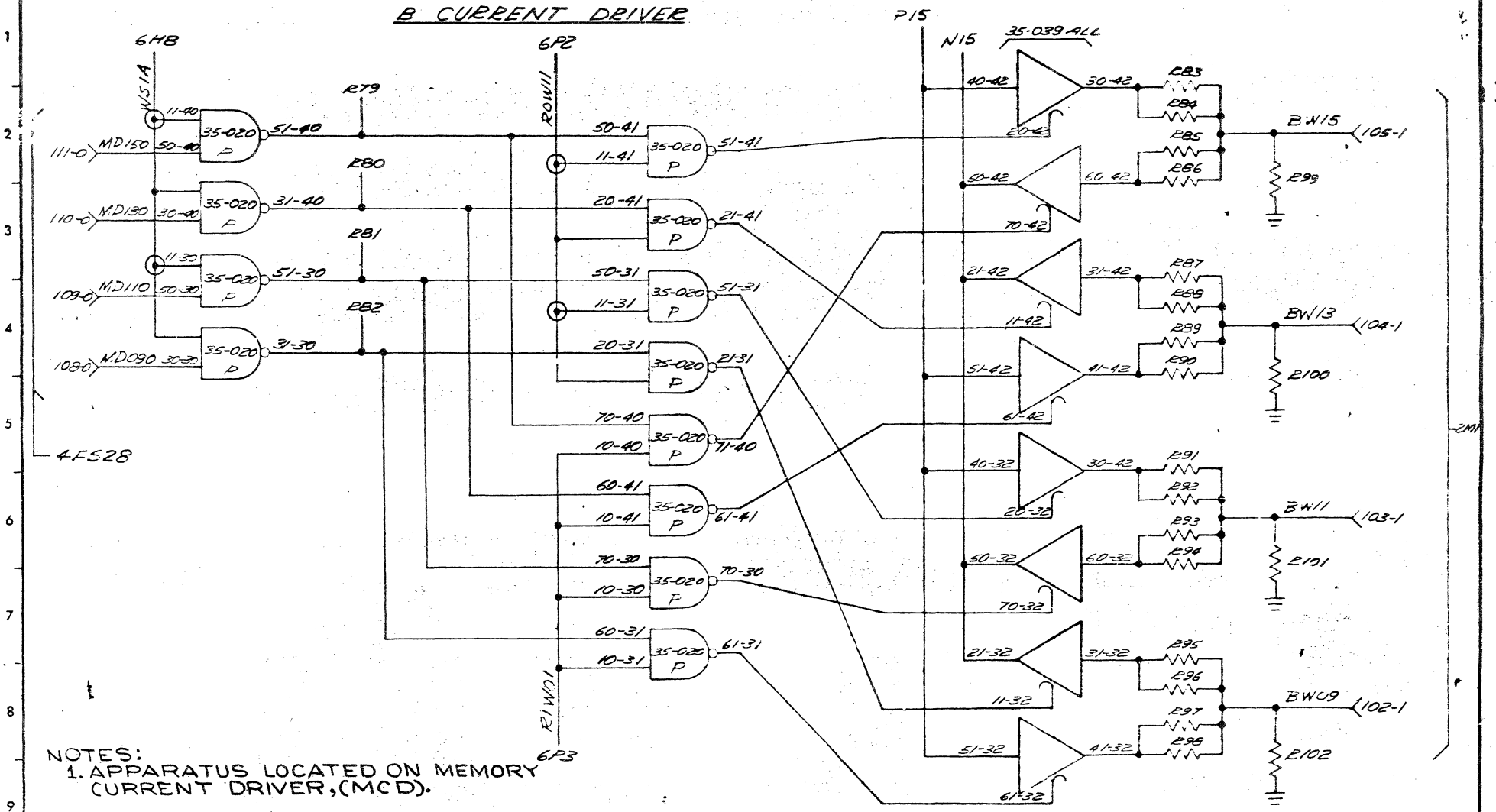
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING –
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30 | FCF

DWG NO (FS50) 70B113009
CONT. ON SHEET 11 SH NO 10

B CURRENT DRIVER



NOTES:
1. APPARATUS LOCATED ON MEMORY CURRENT DRIVER, (MCD).

MADE BY G. Ellsworth JUN. 25, 69
ISSUED JUL 18 1969
APPROVAL E. A. White June 26, 69
DES.
CHKR ND
REV. C

DWG NO (FS50) 70B113009 11 10

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --
APPLIED PRACTICES | SURFACES | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±
SURFACES: √

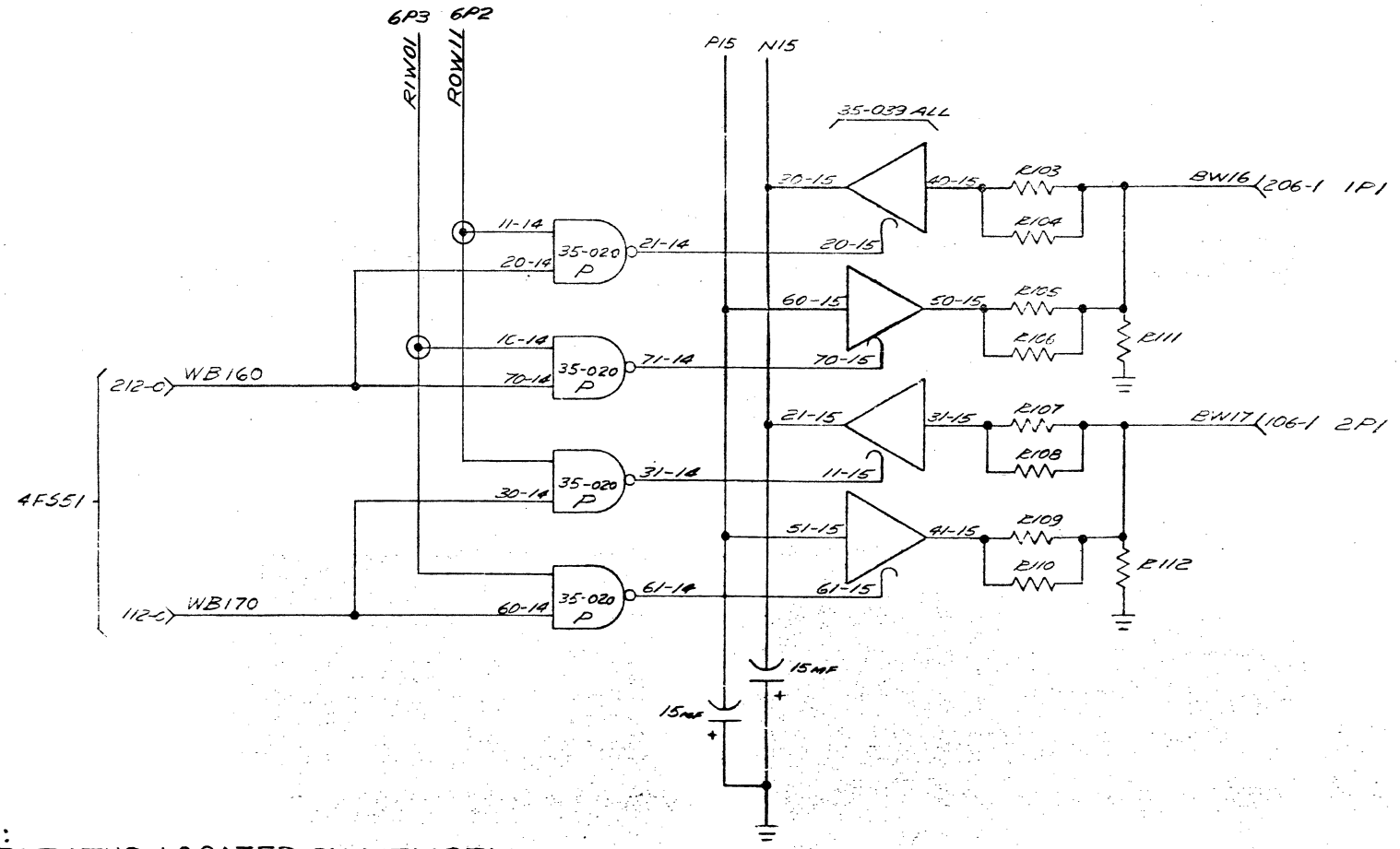
GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30 | FCF

DWG NO (FS50) 70B113009
CONT. ON SHEET 12 SH NO 11

A B C D E F G H J K L M N P R
1 2 3 4 5 6 7 8 9

B CURRENT DRIVER

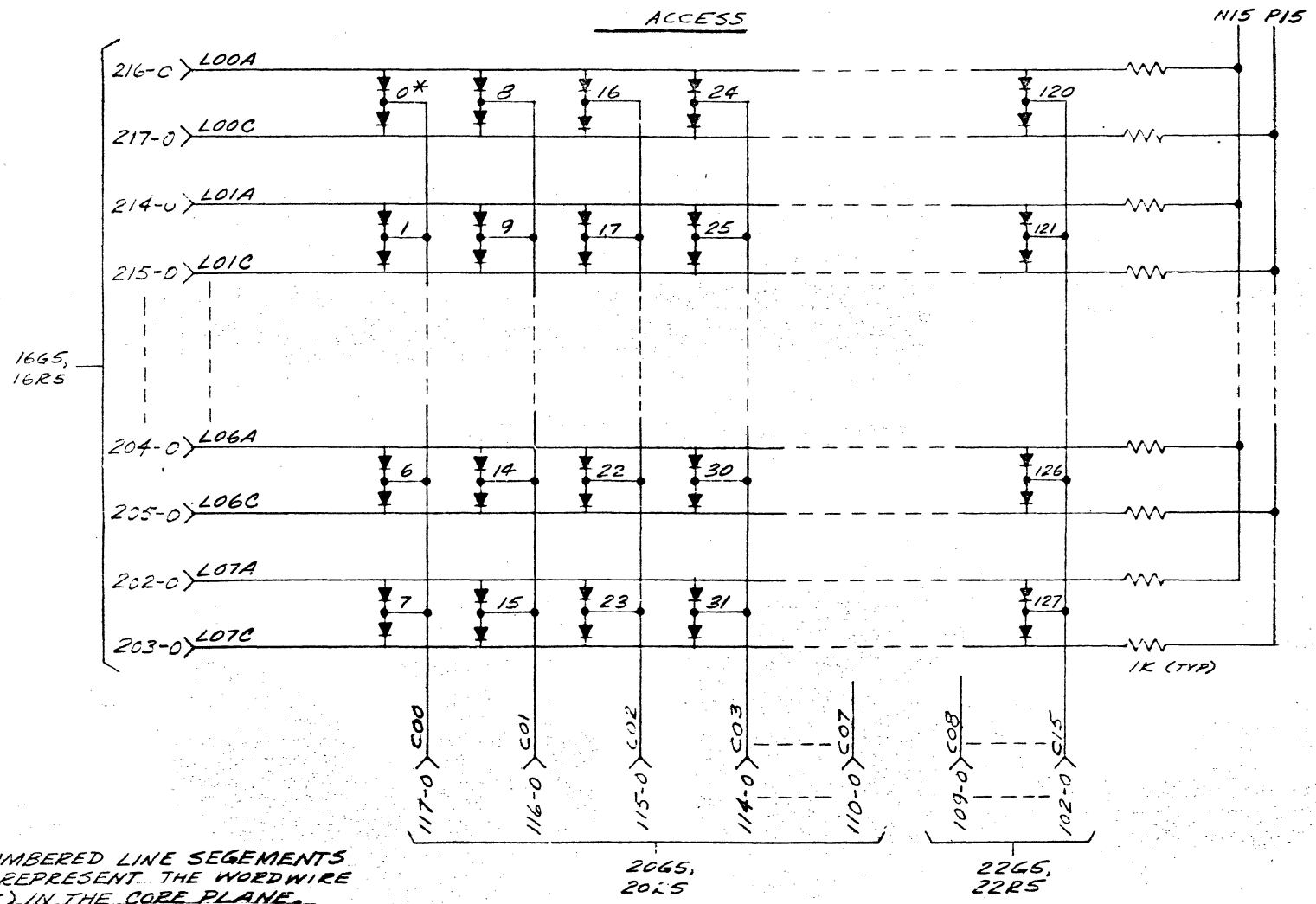


NOTES:
1. APPARATUS LOCATED ON MEMORY CURRENT DRIVER BOARD, (MCD).

MADE BY G. Ellsworth JUN. 25, '69
ISSUED JUL 18 1969
APPROVAL E. A. White June 26, 69
DES
CHKR AD
REV. C

DWG NO (FS50) 70B113009 12 11

DIST.	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING					GENERAL ELECTRIC	TITLE	DWG NO
	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES	PROCESS COMPUTER PHOENIX	FUNCTIONAL SCHEMATIC 4096-16 MEMORY BLOCK FMF GE-PAC 30 | FCF	(FS50) 70B113009
		√	±	±	±			CONT. ON SHEET 13 SH NO 12



* THE NUMBERED LINE SEGEMENTS 0-127 REPRESENT THE WORDWIRE (X-WIRE) IN THE CORE PLANE.

NOTES:
1. APPARATUS LOCATED ON MEMORY "0" BOARD, (MEO).

MADE BY	APPROVAL		REV.		DWG NO
E. Ellsworth JUN. 25, 69	E.G. White June 26, 69	ENGR	C		(FS50) 70B113009
ISSUED JUL 18 1969		CHKR MD			13 12

DIST

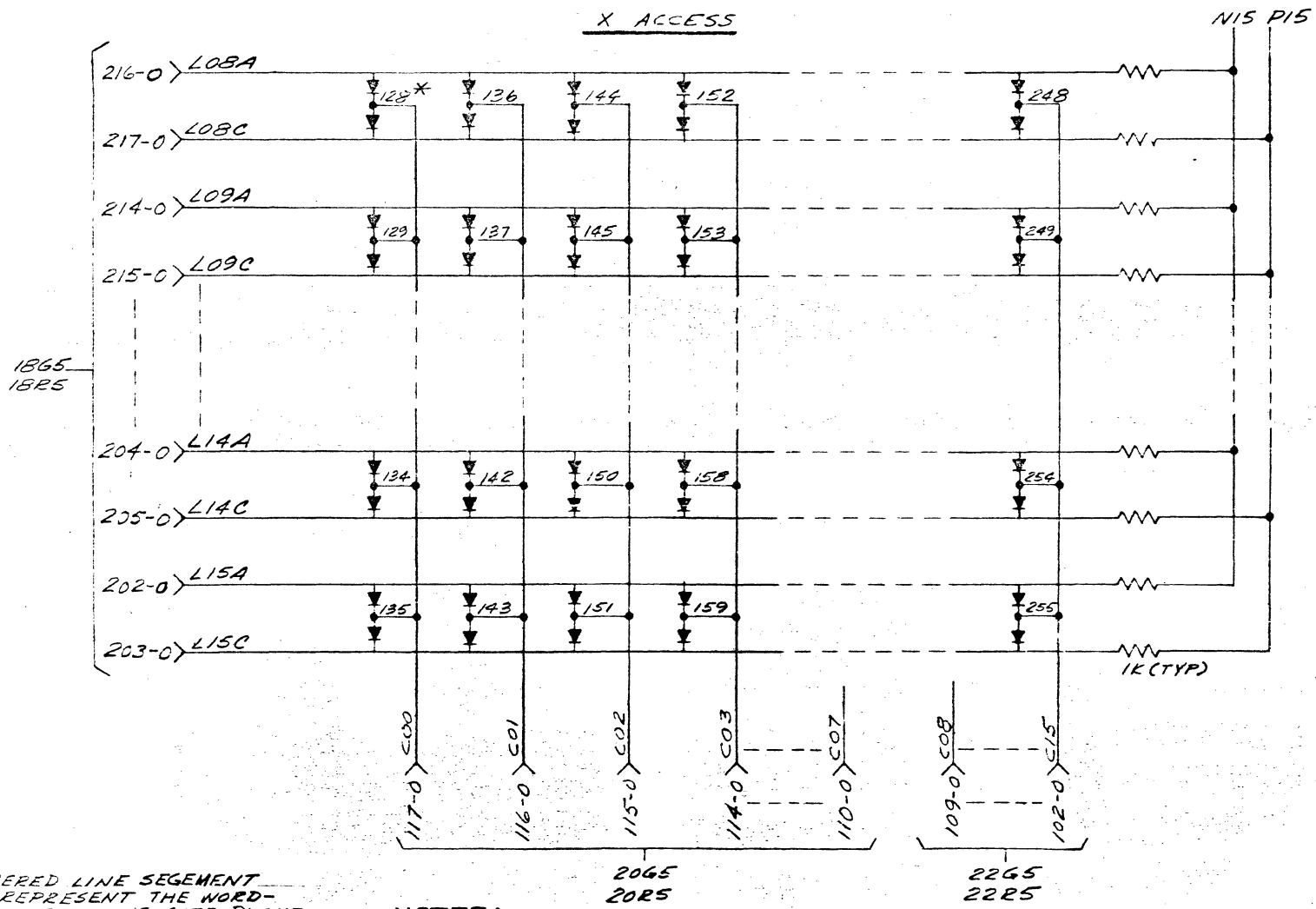
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING				
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS		
		FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30 | FCF

DWG NO (FS50) 70B113009
CONT ON SHEET 14 SH NO 13

X ACCESS



* THE NUMBERED LINE SEGEMENT 128-255 REPRESENT THE WORD-WIRE (X WIRE) IN THE CORE PLANE.

NOTES:
1. APPARATUS LOCATED ON MEMORY BOARD.

MADE BY C. Ellsworth JUN. 25, '69
ISSUED JUL 18 1969
APPROVAL E. A. White June 26 '69
DES
CHKR
REV C

DWG NO (FS50) 70B113009 14 13

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±
SURFACES: √

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

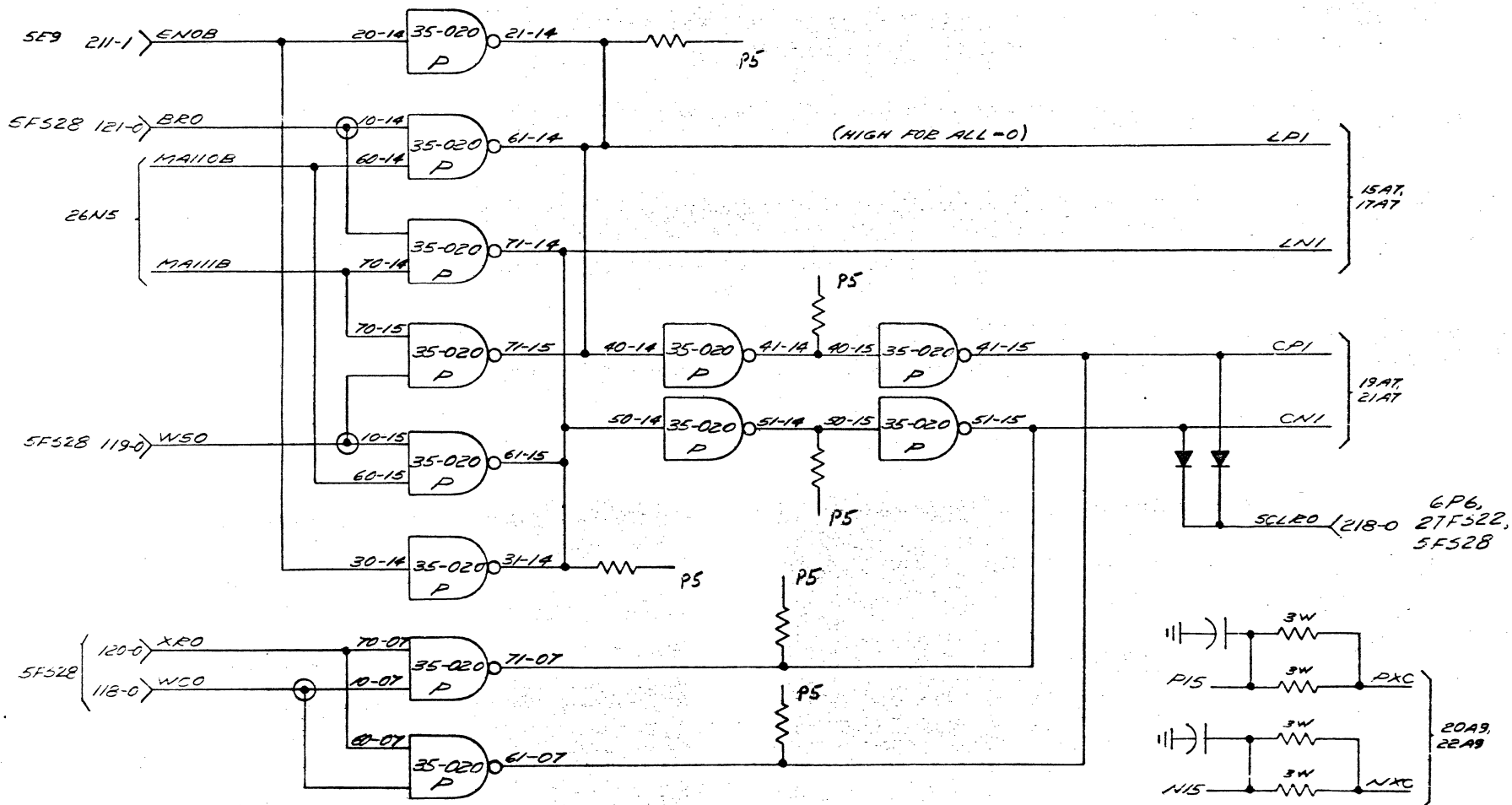
TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30 | FCF

DWG. NO. (FS50) 70B113009
CONT. ON SHEET 15 SH. NO. 14

A B C D E F G H J K L M N P R

1 2 3 4 5 6 7 8 9

X LOGIC



NOTES:
1. APPARATUS LOCATED ON MEMORY SWITCH BOARD, (MSW).

MADE BY	APPROVAL				
C. Ellsworth JUN. 25, 69	E. A. White June 26. 69	DES.		REV.	C
ISSUED JUL 18 1969		CHKD	ND		

DWG NO (FS50) 70B113009 15 14

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING —
APPLIED PRACTICES | SURFACES | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±
SURFACES: √

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30 | FCF

DWG NO (FS50) 70B113009
CONT. ON SHEET 16 SH NO 15

X LINE DECODERS

25M2 MA030B

41-03	00	000		60-03 LOOPO
41-02	00	001		60-02 LOONO
51-03	00	010		70-03 LO1PO
51-02	00	011		70-02 LO1NO
31-03	00	100		10-03 LO2PO
31-02	00	101		10-02 LO2NO
21-03	00	110		20-03 LO3PO
21-02	00	111		20-02 LO3NO

16A5

35-019

20 21 10 11 00 01 20 21

30-03 30-02 11-02 40-03 61-02 11-03 71-03 71-02

41-13	01	000		60-13 LO4PO
41-12	01	001		60-12 LO4NO
51-13	01	010		70-13 LO5PO
51-12	01	011		70-12 LO5NO
31-13	01	100		10-13 LO6PO
31-12	01	101		10-12 LO6NO
21-13	01	110		20-13 LO7PO
21-12	01	111		20-12 LO7NO

16H5

35-019

20 21 10 11 00 01 20 21

30-13 30-12 11-12 40-13 61-12 11-13 71-13 71-12

14R3
- LPI
- LNI
- MA100B
- MA101B
- MA090B
- MA091B
- MA080B
- MA081B

26N3

NOTES:
1. APPARATUS LOCATED ON MEMORY SWITCH BOARD, (MSW).

MADE BY C. Ellsworth JUN. 25, '69
ISSUED JUL 18 1969
APPROVAL E. A. White June 26 69
DES
REV. C

DWG NO (FS50) 70B113009 .16 .15

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS		
		FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30 | FCF

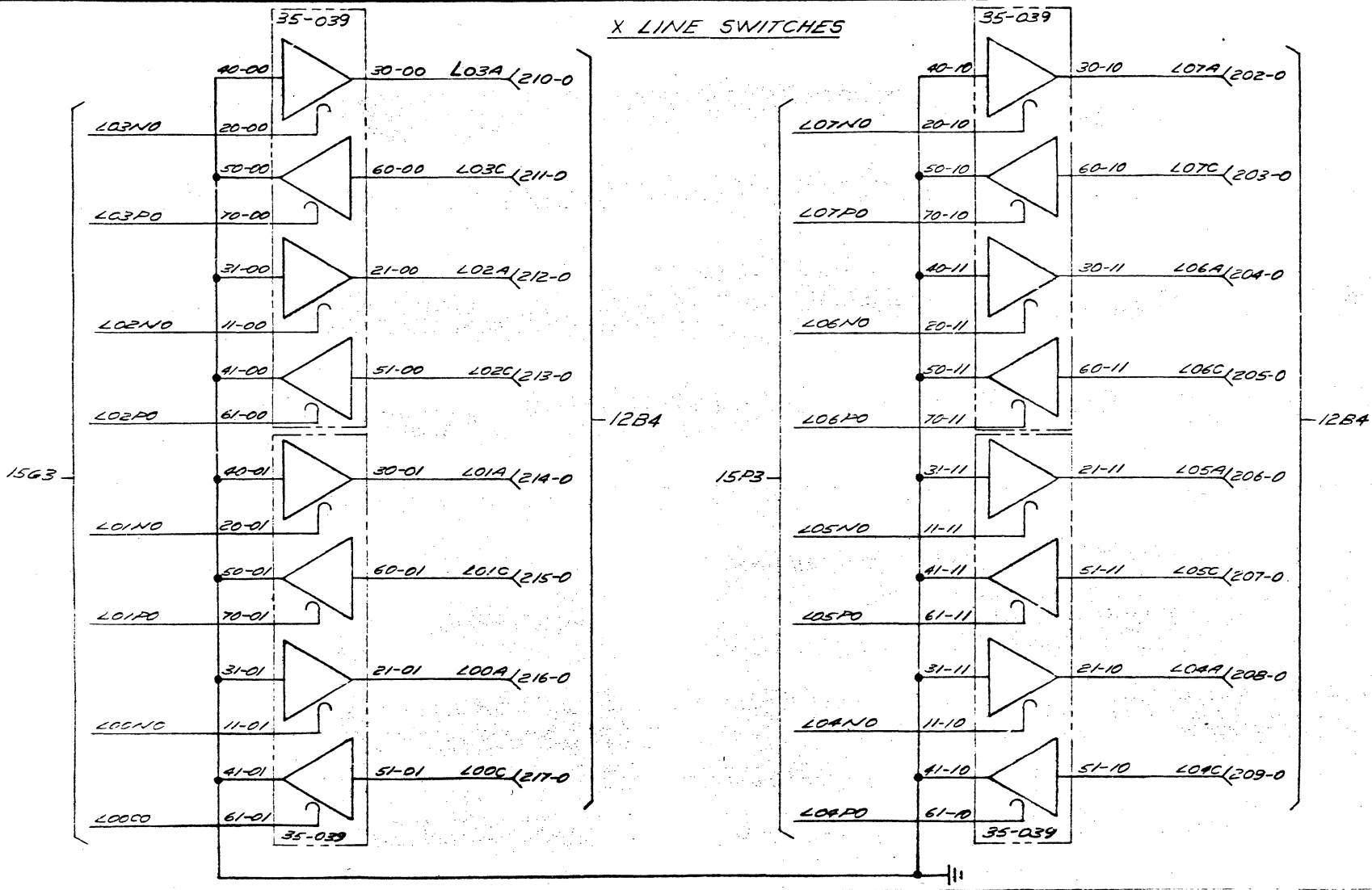
DWG NO (FS50)
70B113009
CONT. ON SHEET 17 SH NO 16

A B C D E F G H J K L M N P R

1 2 3 4 5 6 7 8 9

NOTES:
1. APPARATUS LOCATED ON MEMORY SWITCH BOARD, (MSW).

X LINE SWITCHES



MADE BY	APPROVAL	DES		REV.	
G. Ellsworth JUN. 25, '69	E. A. White				C
ISSUED JUL 18 1969	Time 26. 69	CHKD	NO		

DWG NO (FS50)
70B113009
17 16

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS		
		FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30 | FCF

DWG NO (FS50)
70B113009
CONT ON SHEET 18 SH NO 17

A B C D E F G H J K L M N P R

1

X COLUMN DECODERS

25M2 MA031B

41-23	10	000		60-23 L08P0
41-22	10	001		60-22 L08N0
51-23	10	010		70-23 L09P0
51-22	10	011		70-22 L09N0
31-23	10	100		10-23 L10P0
31-22	10	101		10-22 L10N0
21-23	10	110		20-23 L11P0
21-22	10	111		20-22 L11N0

18A5

35-019

20 21 10 11 00 01 20 21

30-23 30-22 11-22 40-23 61-22 11-23 71-23 71-22

41-33	11	000		60-33 L12P0
41-32	11	001		60-32 L12N0
51-33	11	010		70-33 L13P0
51-32	11	011		70-32 L13N0
31-33	11	100		10-33 L14P0
31-32	11	101		10-32 L14N0
21-33	11	110		20-33 L15P0
21-32	11	111		20-32 L15N0

18H5

35-019

20 21 10 11 00 01 20 21

30-33 30-32 11-32 40-33 61-32 11-33 71-33 71-32

14R3: LP1, LN1, MA100B, MA101B, MA096B

26N3: MA091B, MA080B, MA081B

NOTES:
1. APPARATUS LOCATED ON MEMORY SWITCH BOARD, (MSW).

MADE BY G. Ellsworth JUN. 25, 69
ISSUED JUL 18 1969
APPROVAL June 26, 69
DES.
CHKR. DR
REV. C

DWG NO (FS50)
70B113009
CONT ON SHEET 18 SH NO 17

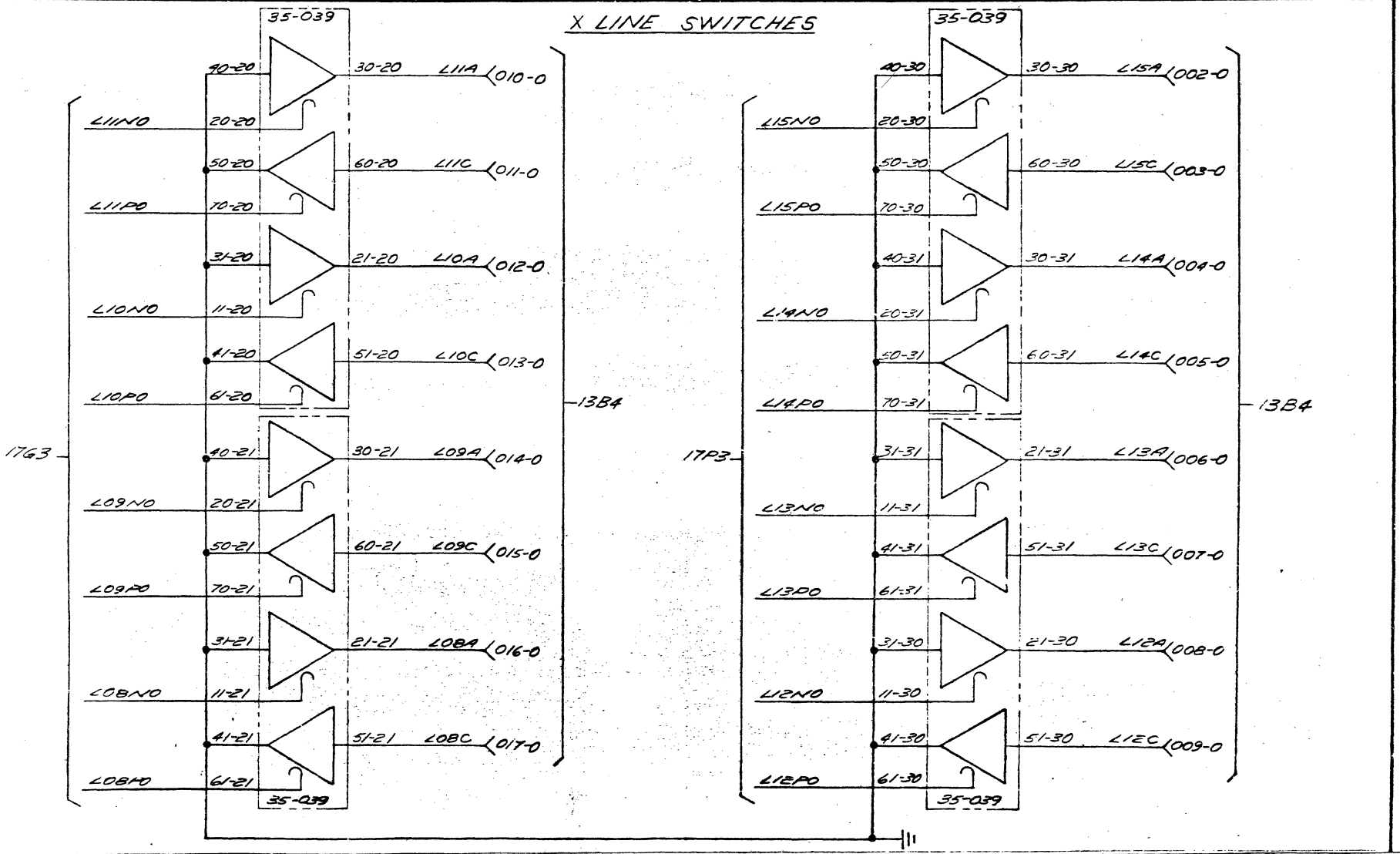
DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING -
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30 | FCF

DWG NO (FS50) 70B113009
CONT ON SHEET 19 SH NO 18



NOTES:
1. APPARATUS LOCATED ON MEMORY SWITCH BOARD, (MSW).

MADE BY G. Ellsworth JUN 25, '69
ISSUED JUL 18 1969
APPROVAL E. A. White June 26, 69
DES.
CHKR DR
REV. C

DWG NO (FS50) 70B113009
CONT ON SHEET 19 SH NO 18

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

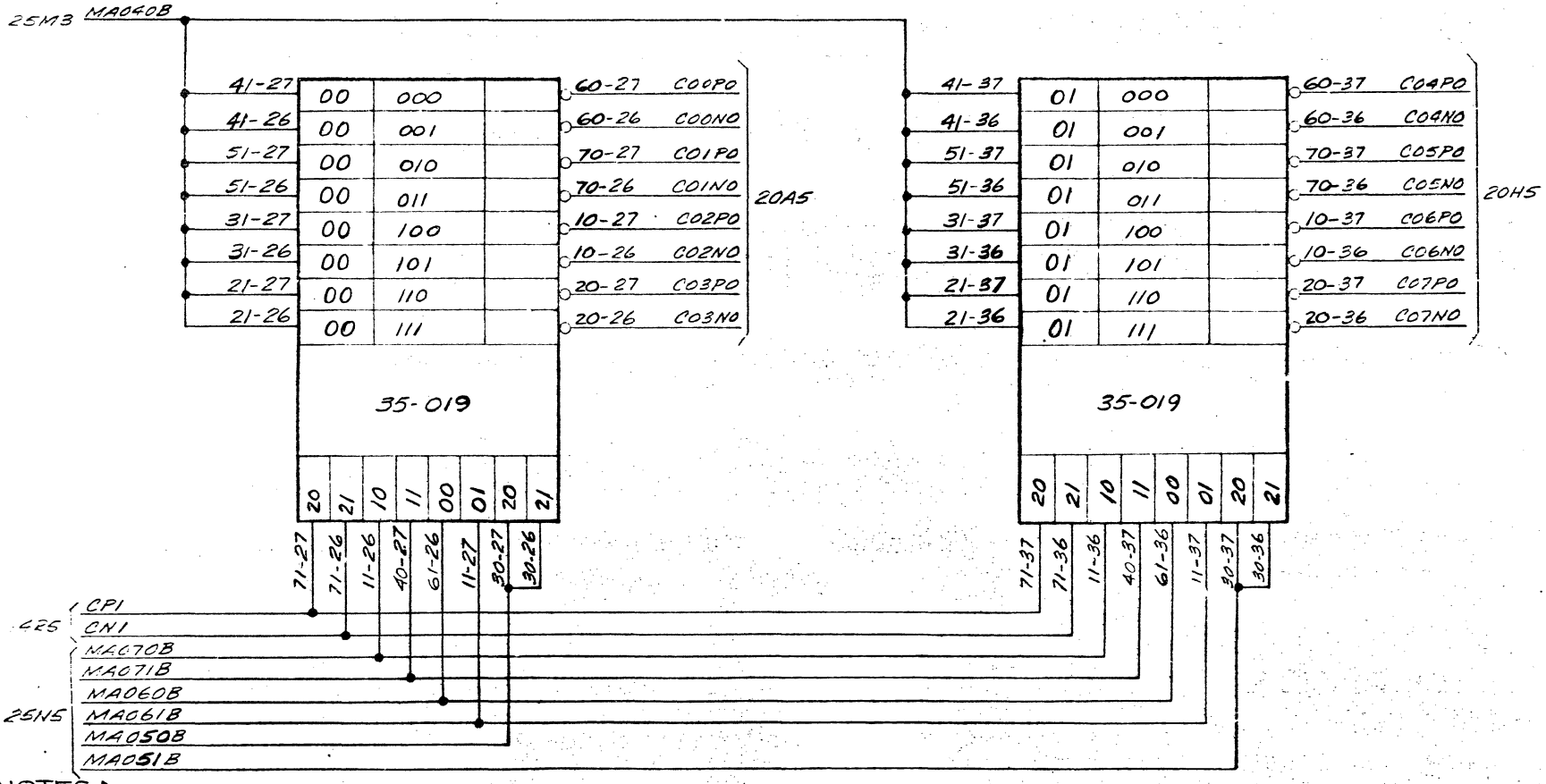
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FOR GE-PAC 30 | FCF

DWG NO (FS50)
70B113009
CONT. ON SHEET 20 SH NO 19

X COLUMN DECODERS



NOTES:
1. APPARATUS LOCATED ON MEMORY SWITCH BOARD, (MSW).

MADE BY	APPROVAL				DWG. NO. (FS50)
E. Ellsworth JUN. 25, 69	E. A. White June 26, 69	DES.	REV. C		70B113009
ISSUED JUL 18 1969		CHKR DR			CONT ON SHT 20 SH NO 19

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

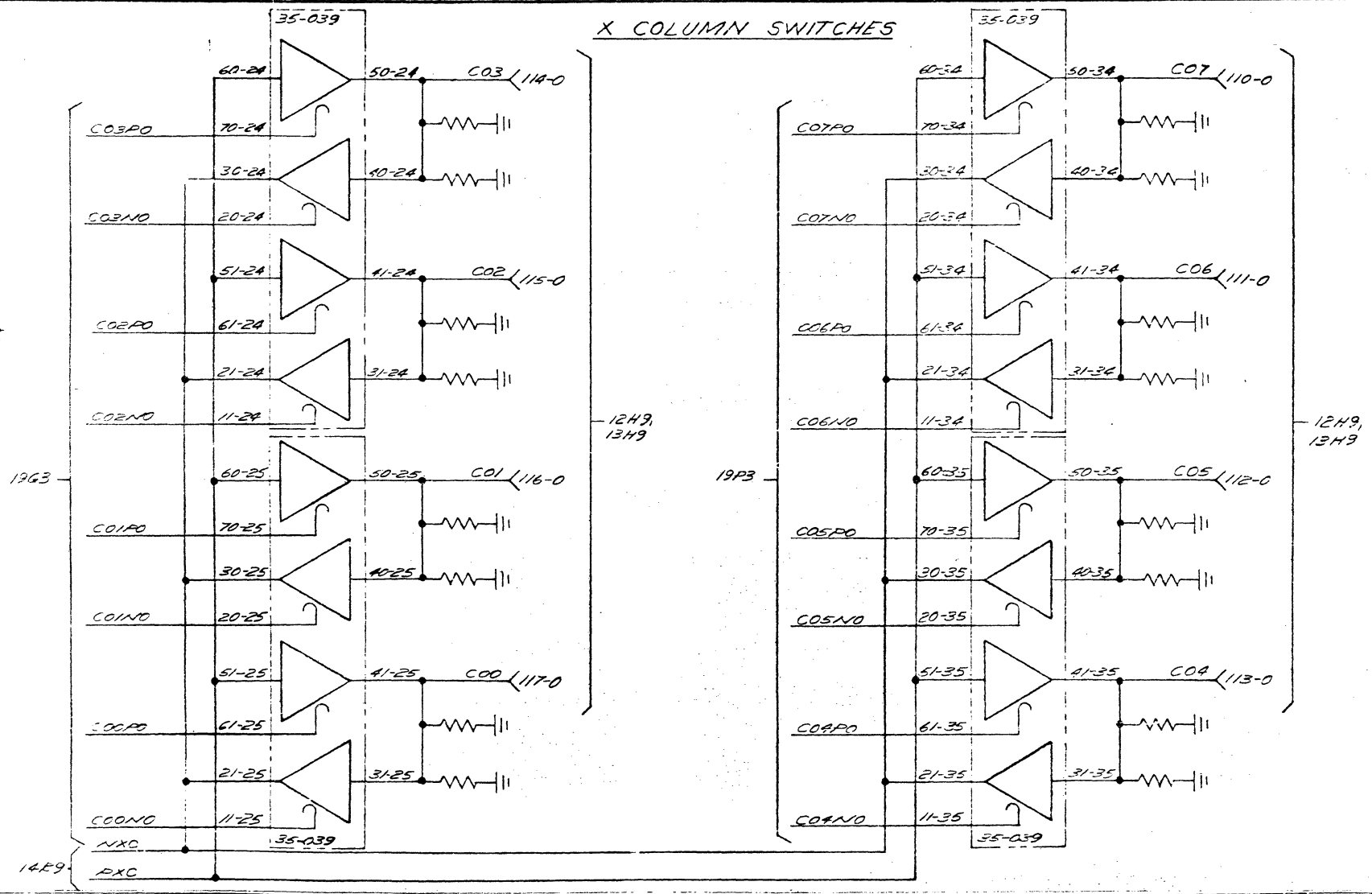
GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30 | FCF

DWG NO (FS50)
70B113009
CONT ON SHEET 21 SH NO 20

NOTES:
1. APPARATUS LOCATED ON MEMORY SWITCH BOARD (MSW).
2. RESISTORS SHOWN ARE ALL 100 Ω, ¼ W.

X COLUMN SWITCHES



MADE BY G. Ellsworth JUN. 25; 69
ISSUED JUL 18 1969

APPROVAL E. A. White June 26, 69

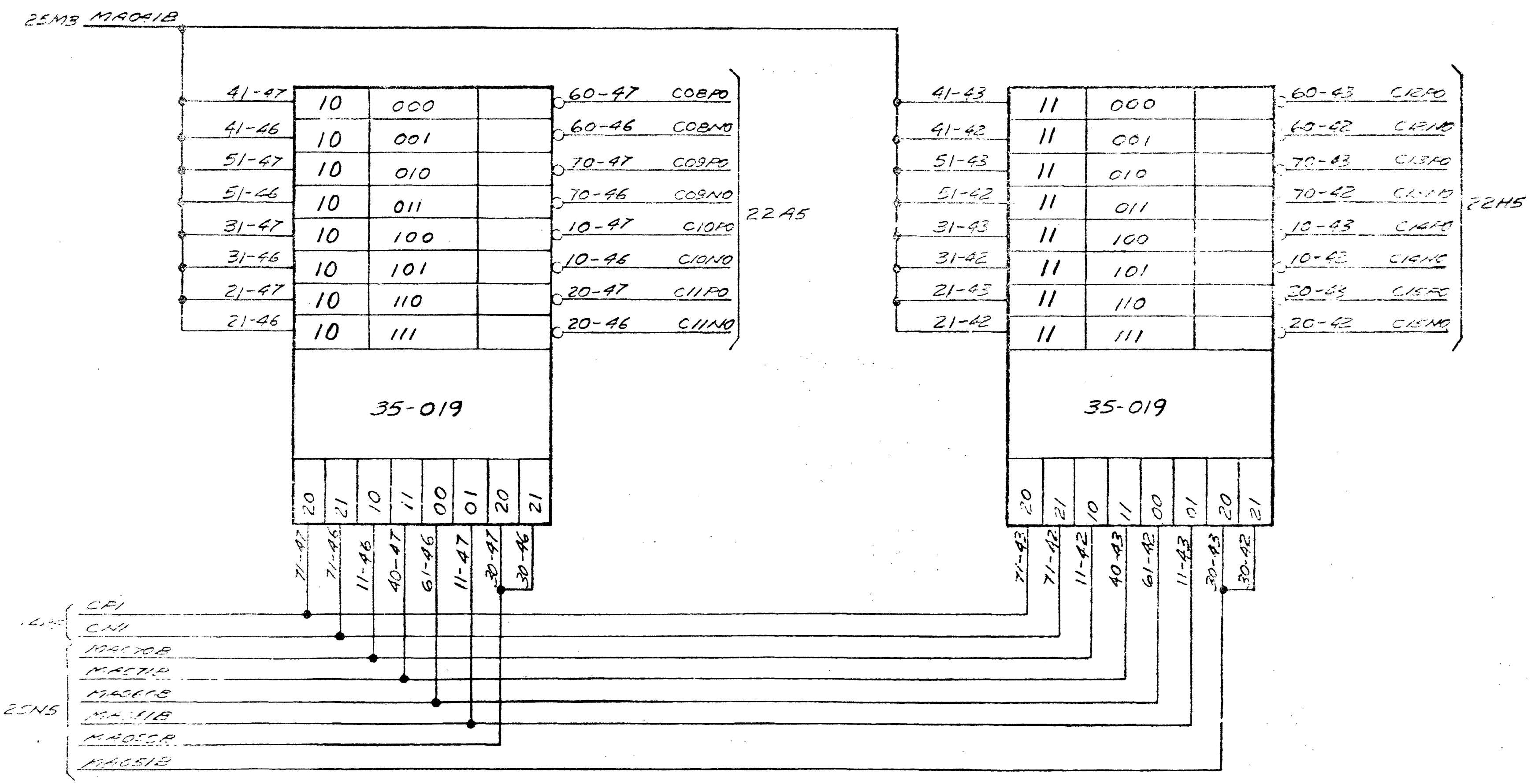
DES.
CHKR. DR

REV. C

DWG NO (FS50)
70B113009
CONT ON SHEET 21 SH NO 20

DIST	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING -					GENERAL ELECTRIC	TITLE	DWG NO
	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES	PROCESS COMPUTER PHOENIX	FUNCTIONAL SCHEMATIC 4096-16 MEMORY BLOCK	(FS50) 70B113009
		√	±	±	±		FMF GE-PAC 30	CONT ON SHEET 22 SH NO 21

X COLUMN DECODERS



NOTES:
1. APPARATUS LOCATED ON MEMORY SWITCH BOARD(MSW).

MADE BY		APPROVAL	DES.		REV.	C	DWG NO
G. Ellsworth	JUN. 25, 69	S. A. White					(FS50) 70B113009
ISSUED	JUL 18 1969	June 26, 69	CHKR	DR			CONT ON SHEET 22 SH NO 21

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

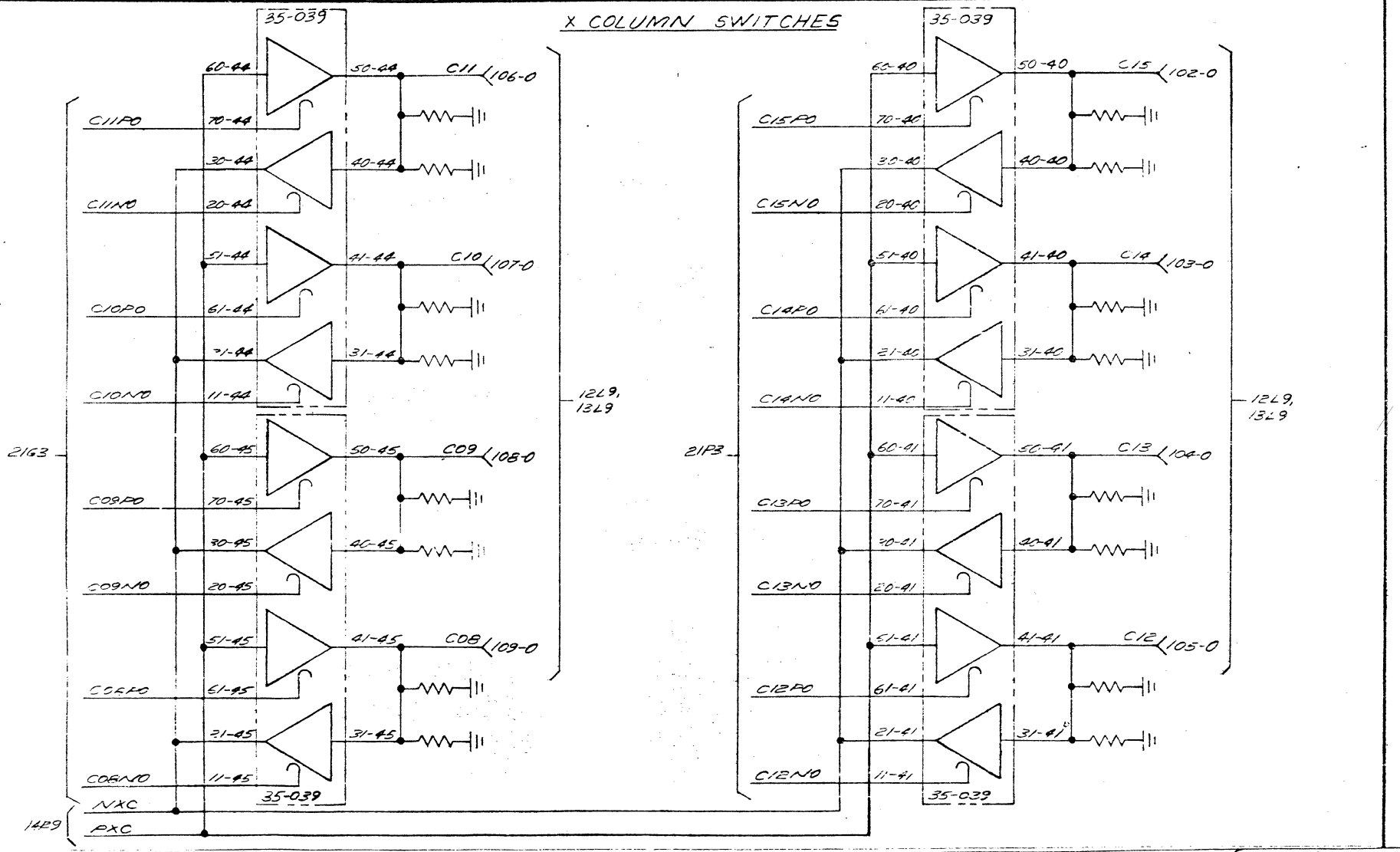
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS		
		FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30 | FCF

DWG NO (FS50)
70B113009
CONT ON SHEET 23 SH NO 22

NOTES:
1. APPARATUS PLATED ON MEMORY SWITCH BOARD, (MSW).
2. RESISTORS SHOWN ARE ALL 100 Ω, ¼ W.



MADE BY
C. Ellsworth JUN. 25, '69

ISSUED
JUL 15 1969

APPROVAL
E. A White
June 26, 69

DES.

CHKR DR

REV. C

DWG NO (FS50)
70B113009
CONT ON SHEET 23 SH NO 22

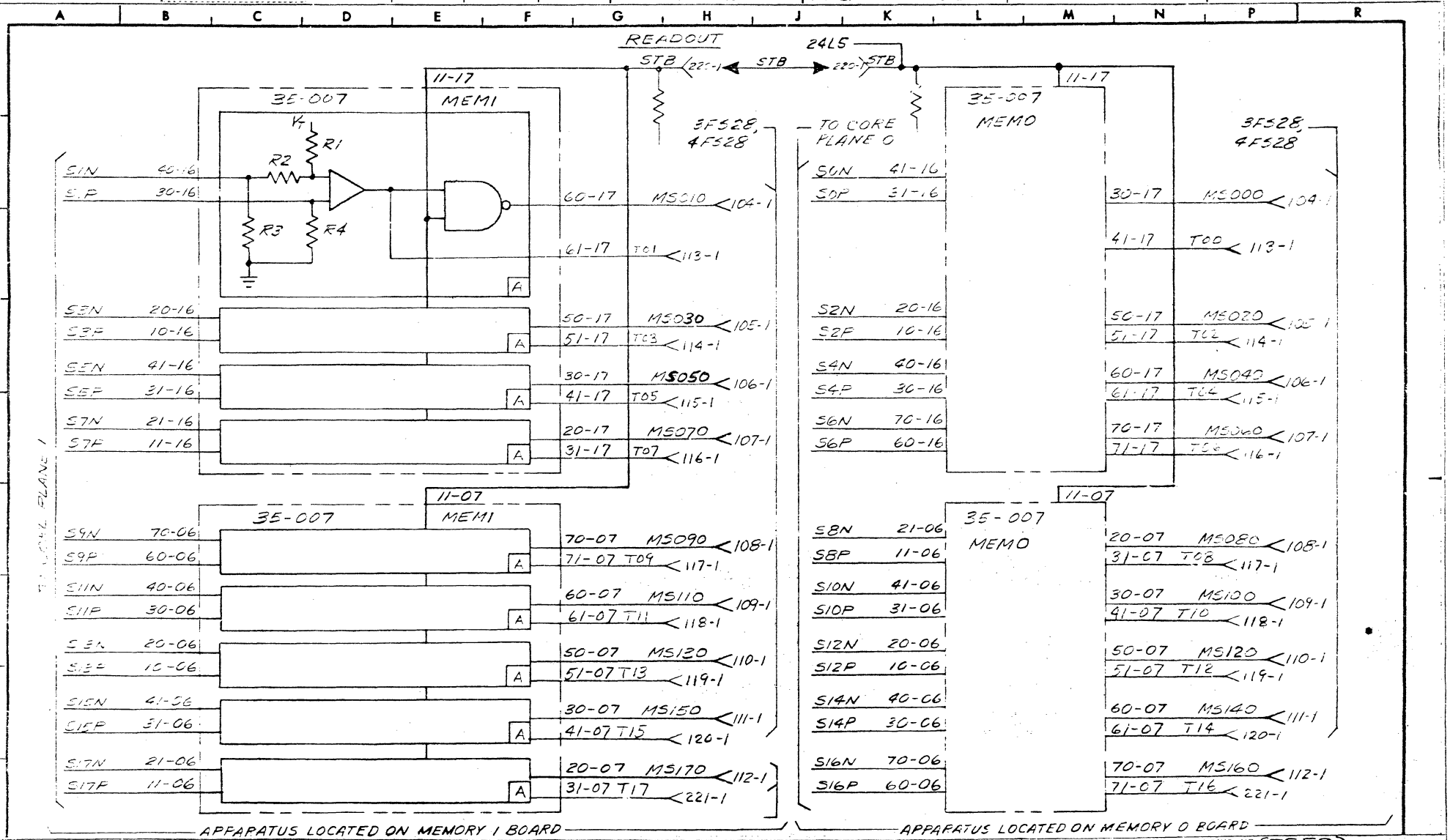
DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING —
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30 | FCF

DWG NO (FS50) 70B113009
CONT ON SHEET 24 SH NO 23



MADE BY E. Ellsworth JUN. 25, '69
ISSUED JUL 18 1969
APPROVAL E.G. White June 26, 69
DES.
CHKR. DR
REV. C

DWG. NO. (FS50) 70B113009
CONT ON SHEET 24 SH NO. 23

DIST.

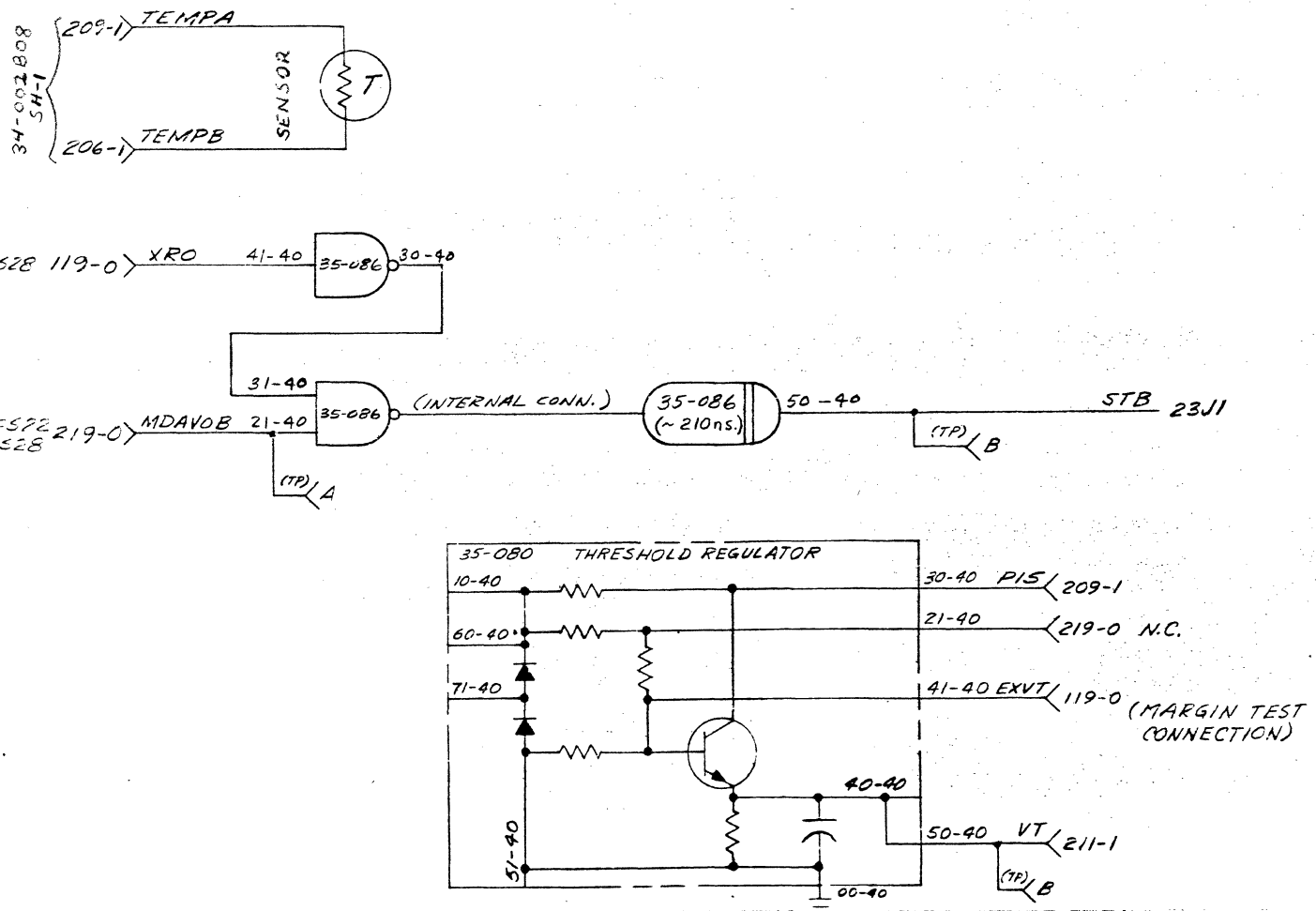
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING :-
APPLIED PRACTICES | SURFACES: √ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30 | FCF

DWG NO (FS50)
70B113009
CONT. ON SHEET 25 SH NO 24

STROBE TIMING



APPARATUS LOCATED ON MEMORY 0 BOARD (ME0)

APPARATUS LOCATED ON MEMORY 1 BOARD (ME1)

MADE BY E Ellsworth JUN. 25, '69
ISSUED JUL 18 1969
APPROVAL E. L. White June 26, 69
DES.
CHKR. DR
REV. C

DWG NO (FS50)
70B113009
CONT ON SHEET 25 SH 24

DIST

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

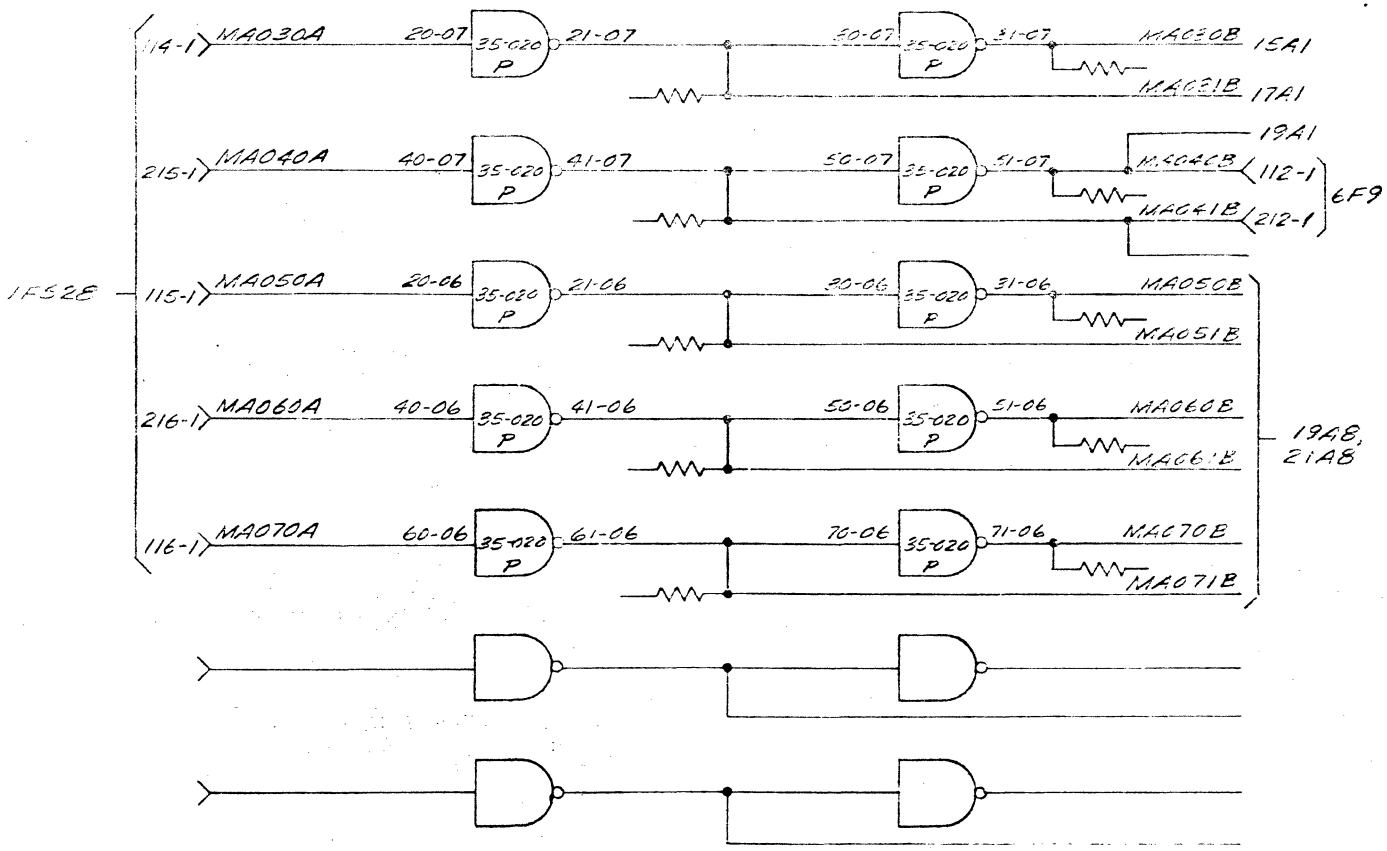
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30

DWG NO (FS50)
70B113009
CONT ON SHEET 26 SH NO 25

ADDRESS BUFFER



NOTES:
1. APPARATUS LOCATED ON MEMORY SWITCH BOARD, (MSW).
2. CONNECT TERMINALS 10 & 11 TO TERMINAL 81 AT MOTHER BOARD POSITIONS 06 & 07 (+5V).

MADE BY C. Ellsworth JUN. 25 '69
ISS 1 JUL 18 1969

APPROVAL E. G. White June 26, 69
DES
CHKR DR

REV. C

DWG NO (FS50)
70B113009
CONT ON SHEET 26 SH NO 25

DIST.

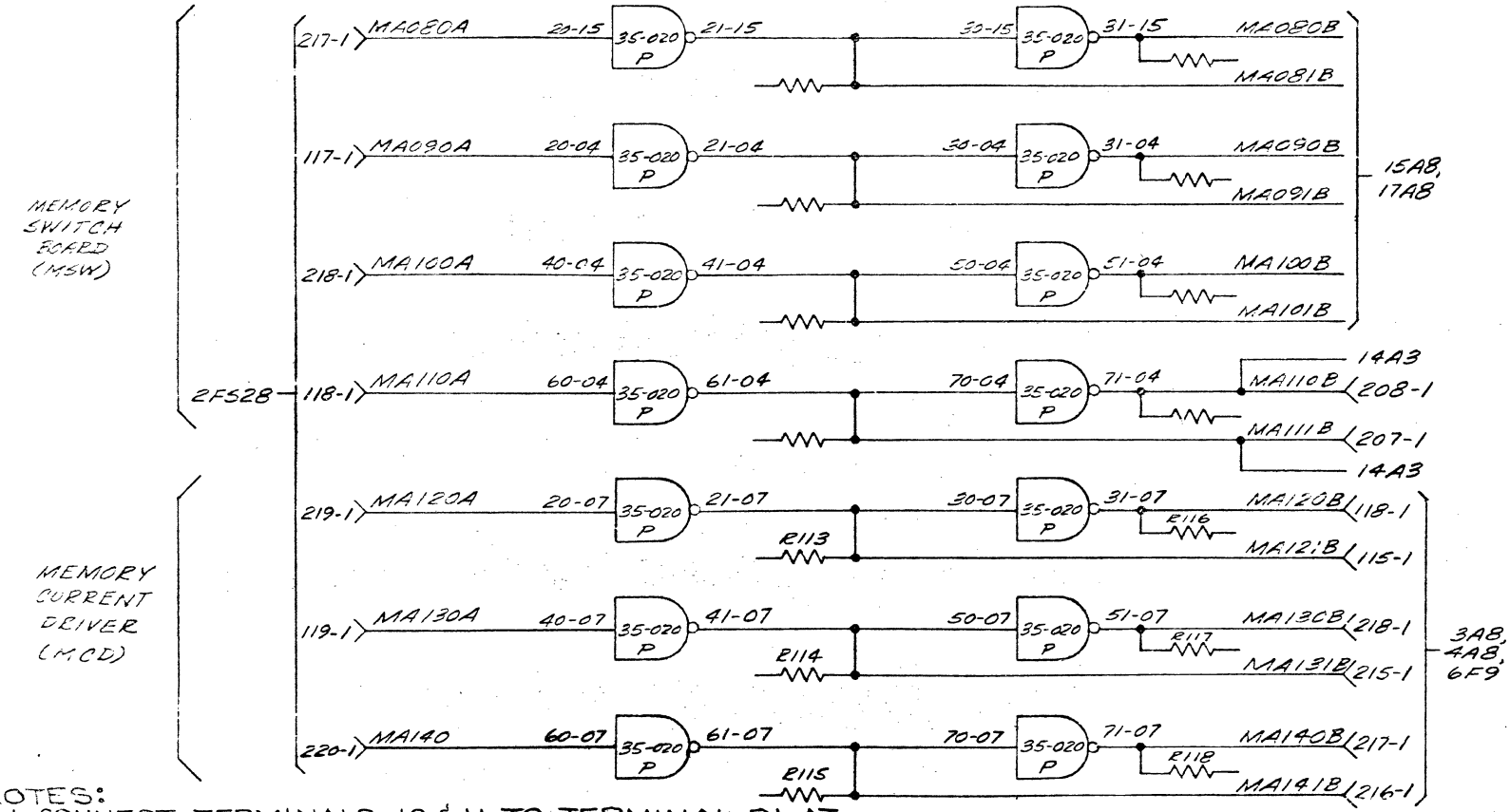
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30 | FCF

DWG NO (FS50)
70B113009
CONT ON SHEET 27 SH NO 26



NOTES:
1. CONNECT TERMINALS 10 & 11 TO TERMINAL 81 AT MOTHER BOARD POSITIONS 04, 07 & 15 (+5).

MADE BY C. Ellsworth JUN. 25, '69
ISSUED JUL 18 1969

APPROVAL E.G. White DES.
June 26, 69 CHKR. DR

REV. C

DWG NO (FS50)
70B113009
CONT ON SHEET 27 SH NO 26

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
4096-16 MEMORY BLOCK
FMF GE-PAC 30 | FCF

DWG NO (FS50) 70B113009
CONT ON SHEET F SH NO 27

BACK PANEL MAP FS50 — FS28

CONN POS	00			01			02			03			C5			06		
MCT 4. BD	MPP			MCD			MEI (ROM TEMP)			MEO			M&W (ROM SW)			MSFC		
VERT. POS	HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS		
	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2
22		P5	GND		P5	GND		P5	GND		P5	GND		P5	GND		P5	GND
21		MC2	MC1					P15	T17		P15	T16		P15	N15	MC2	MC1	
20		MA15OA	MA14OA			MA14OA		T15	STB		T14	STB				MA15OA	MA14OA	5151
19		MA13OA	MA12OA		MA13OA	MA12OA		T13	MA12CB		T12	MA12CB				MA13OA	MA12OA	5141
18		MA11OA	MA10OA		MA12OB	MA13OA		T11	MA13CA		T10	MA13CB		MA11CA	MA12CA	MA11OA	MA10OA	5131
17		MA09OA	MA08OA			MA14OB		T09	MA14CB		T08	MA14CB		MA09CA	MA8CA	MA9OA	MA8OA	5121
16		MA07OA	MA06OA			MA14IB		T07	MA14IB		T06	MA14IB		MA07CA	MA6BA	MA7OA	MA6OA	5111
15		MA05OA	MA04OA		MA12IB	MA13IB		T05	MA13IB		T04	MA13IB		MA05CA	MA04CA	MA5OA	MA4OA	5101
14		MA03OA	MA02OA		MA13CA	MA12OA		T03	MA12IB		T02	MA12IB		MA03OA		MA3OA	MA2OA	5091
13		MA01OA	MA00OA		MA01OA	MA14CA		T01	ENI		T00	ENI				MA01OA	MA14CA	5071
12		MS170	MS160		ENCA	ENI		MS170	N15(6)		MS160	N15(6)		MA14CB	MA04IB			5061
11		MS150	MS140		MA14CB	MA14IB		MS150	VT		MS140	VT			ENCB	MS150	MS140	5051
10		MS130	MS120		ENCB			MS130	P15 (12)		MS120	P15 (12)				MS130	MS120	5041
09		MS110	MS100					MS110	P15 (VT)		MS100	TEMPA				MS110	MS100	5031
08		MS090	MS080					MS090	VT		MS080					MS090	MS080	5021
07		MS070	MS060					MS070			MS060					MS070	MS060	5011
06		MS050	MS040		BW17	BW16		MS050	N.C.(31)		MS040	TEMPB				MS050	MS040	5001
05		MS030	MS020		BW15	BW14		MS030	N.C.(16.2)		MS020	ENCA				MS030	MS020	
04		MS010	MS000		BW13	BW12		MS010			MS000	ENCB				MA01O	MS000	LMALO
03		MC4	MC3		BW11	BW10		BW17	BW15		BW16	BW14				MC4	MC3	LMAHO
02		OVRAI	PROLO		BW09	BWOB		BW13	BW11		BW12	BW10				OVRAI	PROLO	
01		STWO	CWRO		BW07	BW06		BW09	BW07		BW08	BW06				STWO	CWRO	
00		P5	GND						GND			GND			GND		P5	GND
22		P5	GND						GND			GND			GND		P5	GND
21		BRO	CLOE		BW05	BW04		BW03	BW05		BW02	BW04		BRO		STRTC	SRO	CLOE
20		XRO	CPFH		BW03	BW02			BW01			BW00		XRO		MLEC(16)	PRO	LMALO
19		NSO	CPFL		BW01	BW00		EXVT	N.C.(21)		XRO	MDAVOB		WSO		WRO	MSO	LMDHO
18		WCO	PFHI					GND	GND		GND	GND		NCO	SCLRO	SCLRO	WCO	MCLO
17		MDAVOB	PFLI		GND	GND		C00	L08C		C00	L00C	L08C	C00	L01C	MDAVOB	MDAVOA	LMDHO
16		MENI	PFHO		MENI	ROW11		C01	L08A		C01	L00A	L08A	C01	L00A	MBYIA		B150
15		MDHRO	PFLO		ROW01	WSO		C02	L09C		C02	L01C	L09C	C02	L01C	SHARO	MDHRO	B140
14		SHARO	MS		BRO	WCO		C03	L09A		C03	L01A	L09A	C03	L01A	MENI	CPARO	B130
13		CPAEC	SCLRO			SCLRO		C04	L10C		C04	L02C	L10C	C04	L02C		MDLRO	B120
12		MD170	MD160		WD170	WD160		C05	L10A		C05	L02A	L10A	C05	L02A			B110
11		MD150	MD140		MD150	MD140		C06	L11C		C06	L03C	L11C	C06	L03C	MD150	MD140	B100
10		MD130	MD120		MD130	MD120		C07	L11A		C07	L03A	L11A	C07	L03A	MD130	MD120	B090
09		MD110	MD100		MD110	MD100		C08	L12C		C08	L04C	L12C	C08	L04C	MD110	MD100	B080
08		MD090	MD080		MD090	MD080		C09	L12A		C09	L04A	L12A	C09	L04A	MD090	MD080	B070
07		MD070	MD060		MD070	MD060		C10	L13C		C10	L05C	L13C	C10	L05C	MD070	MD060	B060
06		MD050	MD040		MD050	MD040		C11	L13A		C11	L05A	L13A	C11	L05A	MD050	MD040	B050
05		MD030	MD020		MD030	MD020		C12	L14C		C12	L06C	L14C	C12	L06C	MD030	MD020	B040
04		MD010	MD000		MD010	MD000		C13	L14A		C13	L06A	L14A	C13	L06A	MD010	MD000	B030
03		MS170	PPHO					C14	L15C		C14	L07C	L15C	C14	L07C		PDWO	B020
02		MS160	PPLO					C15	L15A		C15	L07A	L15C	C15	L07A			B010
01		PDWO	MBYIA		P15	N15		P15	N15		P15	N15		P15	N15			B000
00		P5	GND			GND			GND			GND		P5	GND		P5	GND

MADE BY C. Ellsworth JUN. 25, '69
ISSUED JUL 18 1969

APPROVAL E. A. White June 26, 69
DES
CHKR OR

REV. C

DWG NO (FS50) 70B113009
CONT ON SHEET F SH NO 27

GENERAL ELECTRIC

PROCESS COMPUTERS
PHOENIX ARIZONA

TITLE FUNCTIONAL SCHEMATIC.
MEMORY PARITY & PROTECT

DRAWING NUMBER 70B113010 | CONT. 0A | PAGE 0
FIRST MADE FOR GE-PAC 30
(FS51)

REVISION STATUS

RF	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
C	ISSUE				

REISSUED

A	Issued										

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME

REISSUED

(FS51)

MADE BY B. Howard 24 JUNE '69
ISSUED July 18, 1969
APPROVAL E. G. White June 25, 69
REV. C

DWG. NO. 70B113010 | CONT. 0A | PAGE 0
PRINTS TO: K7-08

PCE 2981

DIST	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING					GENERAL ELECTRIC	TITLE	DWG NO (FS51)
	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACH'ND DIMENS'NS FRACTIONS	DECIMALS	ANGLES	PROCESS COMPUTER PHOENIX	FUNCTIONAL SCHEMATIC MEMORY PARITY & PROTECT	70B113010
		√	±	±	±	FMF GE-PAC 30 | FCF	CONT. ON SHEET | SH NO 0A	

SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
SHEET INDEX SUPPORTING INFORMATION	0A	1	2																		
MEMORY PROTECT	1	1	2																		
	2	1	1																		
MEMORY PARITY	3	1	2																		
	4	1	1																		
	5	1	1																		
	6	1	1																		
BACK PANEL MAP	7	1	1																		
BLOCK DIAGRAM	8	1	1																		
ISSUE DATE		12-20-68	2-28-69																		

SUPPORTING INFORMATION

CATEGORY	PART NO.
MOTHER BOARD	
MEM. PARITY & PROTECT	32-087201
MEM. PARITY	32-087F01201
MEM. PROTECT	32-087F02201

SHEET INDEX NOTES:

1. CHANGES ON THIS DRAWING SHALL REQUIRE ONLY THE REISSUE OF SHEETS AFFECTED.
2. THE ISSUE OF THIS SHEET SHALL DETERMINE THE LATEST ISSUE OF THIS DRAWING.

MADE BY	APPROVAL	DES	REV.							DWG NO (FS51)
[illegible] and 24 JUNE 69	E. A. White June 25, 69	CHKR DR	C							70B113010
ISSUED JUL 18 1969										CONT ON SHEET 1 SH NO 0A

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --
APPLIED PRACTICES | SURFACES | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

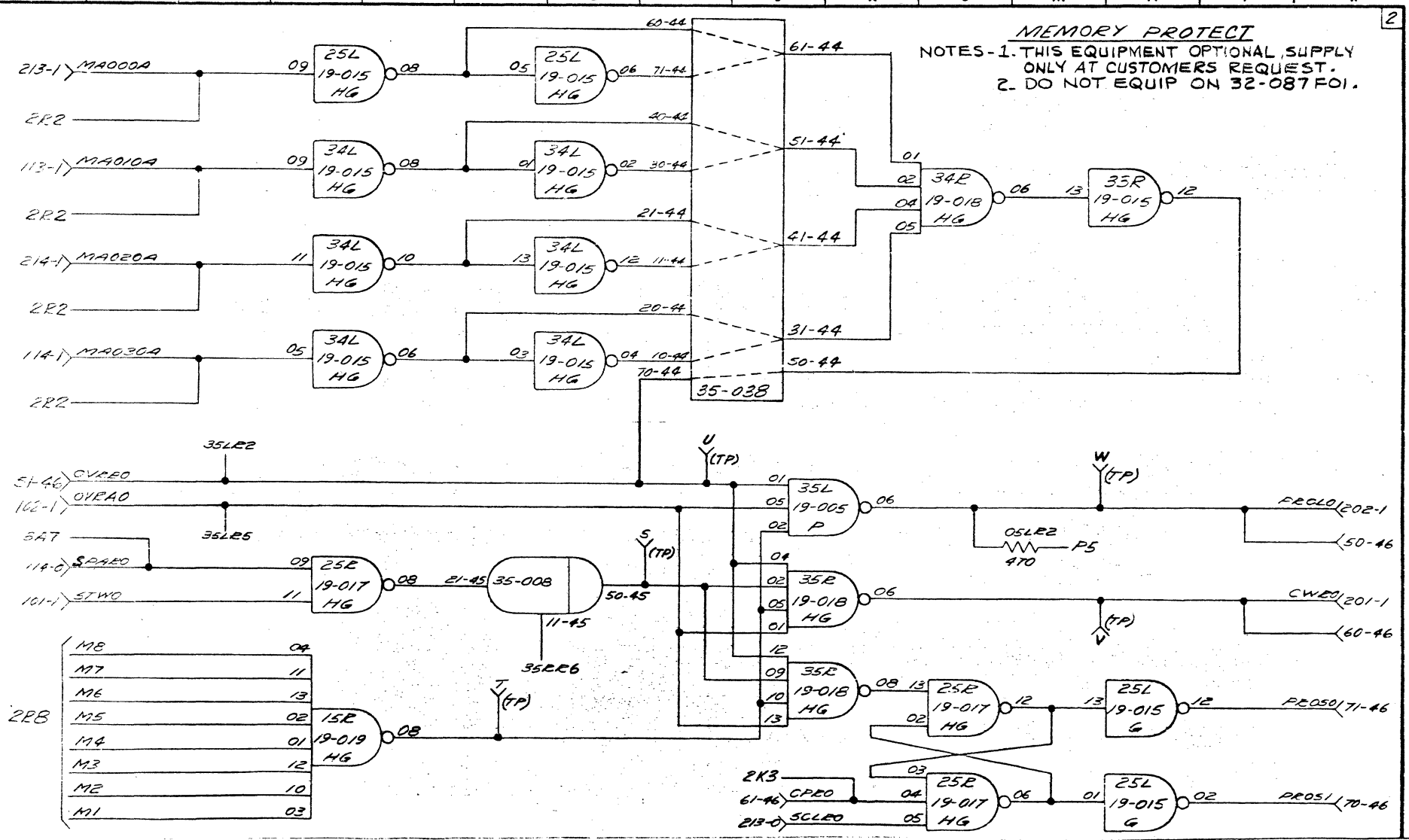
GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC.
MEMORY PARITY & PROTECT
FMF GE-PAC 30 | FCF

DWG NO. (FS51) 70B113010
CONT. ON SHEET 2 SH NO. 1

MEMORY PROTECT

NOTES - 1. THIS EQUIPMENT OPTIONAL, SUPPLY ONLY AT CUSTOMERS REQUEST.
2. DO NOT EQUIP ON 32-087 F01.



MADE BY	APPROVAL					DWG NO. (FS51)
M. Howard 24 JUNE '69	E.G. White June 25, 69	DES.		REV.	C	70B113010
ISSUED JUL 18 1969		CHKR.	DR			CONT ON SHEET 2 SH NO. 1

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING —

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS		
		FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC.
MEMORY PARITY & PROTECT
FMF GE-PAC 30 | FCF

DWG NO. (FS51)
70B113010
CONT. ON SHEET 3 SH NO. 2

MEMORY PROTECT

NOTES:
1. CAPACITORS ARE NOT NORMALLY EQUIPPED. USE 22PF CAPACITORS IF EXTERNAL BLOCK LEADS EXCEED 4 FT..
2. DO NOT EQUIP ON 32-087F01.

K2

PA3 PA2 PA1 PA0 (TP) Y

06R 19-015 HG
06L 19-015 HG
06F 19-015 HG

E1 PA0 30-07 PA1 60-07 PA2 50-07 PA3 40-07 CPRO 10-07

IJ9 35-038

71-07 MA000A
70-07 MA001A
61-07 MA002A
51-07 MA003A
41-07 MA004A
31-07 MA005A
21-07 MA006A
11-07 MA007A
20-07 MBY.A

1A2, 1A3, 1A4, 1A5
215-1
115-1
216-1
116-1
116-0

CONNECT AS SHOWN FOR 1K BYTE BLOCK SIZE

16L 19-001 G
16R 19-001 G
26L 19-001 G
26R 19-001 G
27R 19-001 G
27L 19-001 G
17R 19-001 G
17L 19-001 G

16LR1 36LR3 16RR1 15RR6 26LR1 25LR2 36RR2 25RR6 37RR2 37RR6 37RR4 37RR8 36LR6 17RR4 27LP1 17LR6

1A8

MADE BY	APPROVAL	DES.	REV.	DWG NO. (FS51)
E. Howard 24 JUNE '69	E.A. White June 25, 69	CHKR. DR	C	70B113010
ISSUED JUL 18 1969				CONT ON SHEET 3 SH NO. 2

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—
APPLIED PRACTICES | SURFACES ✓ | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC.
MEMORY PARITY & PROTECT
FMF GE-PAC 30 | FCF

DWG. NO (FS51) 70B113010
CONT. ON SHEET 4 SH. NO. 3

MEMORY PARITY

22RR2

102-C MS160
6R3 BYP160 (TP) J
22R 19-014 FF
MD161 G (TP)
MD160 5A4
119-0 WS0 22L 19-003 G
113-0 CPAR0 21L 19-016 HG
35-008 50-41 21-41 11-41
42LR2
(TP) C
115-0 MDHR0
1A6 SPAR0 21L 19-016 HG (TP) E
4R3 BYP170 (TP) K
MD170 5A8
MD171 (TP) F
103-C MS170
22RR5

13R 19-007 FF
CPFH 220-0
PFF0
PFH0 216-0
MPF0
PFH1 218-0
WD160 212-0
PPH0 203-0
PPL0 202-0
WD170 112-0
12R 19-007 FF
PLF1 217-0
PLF0 215-0
CPFL 219-0

NOTES:
1. DO NOT EQUIP ON 32-087F02.

MADE BY	APPROVAL	DES.	REV.		DWG. NO (FS51)
B Howard 24 JUNE '69	E. G. White June 25, 69	CHKR. DR	C		70B113010
ISSUED JUL 18 1969					CONT ON SHEET 4 SH NO. 3

DIST.

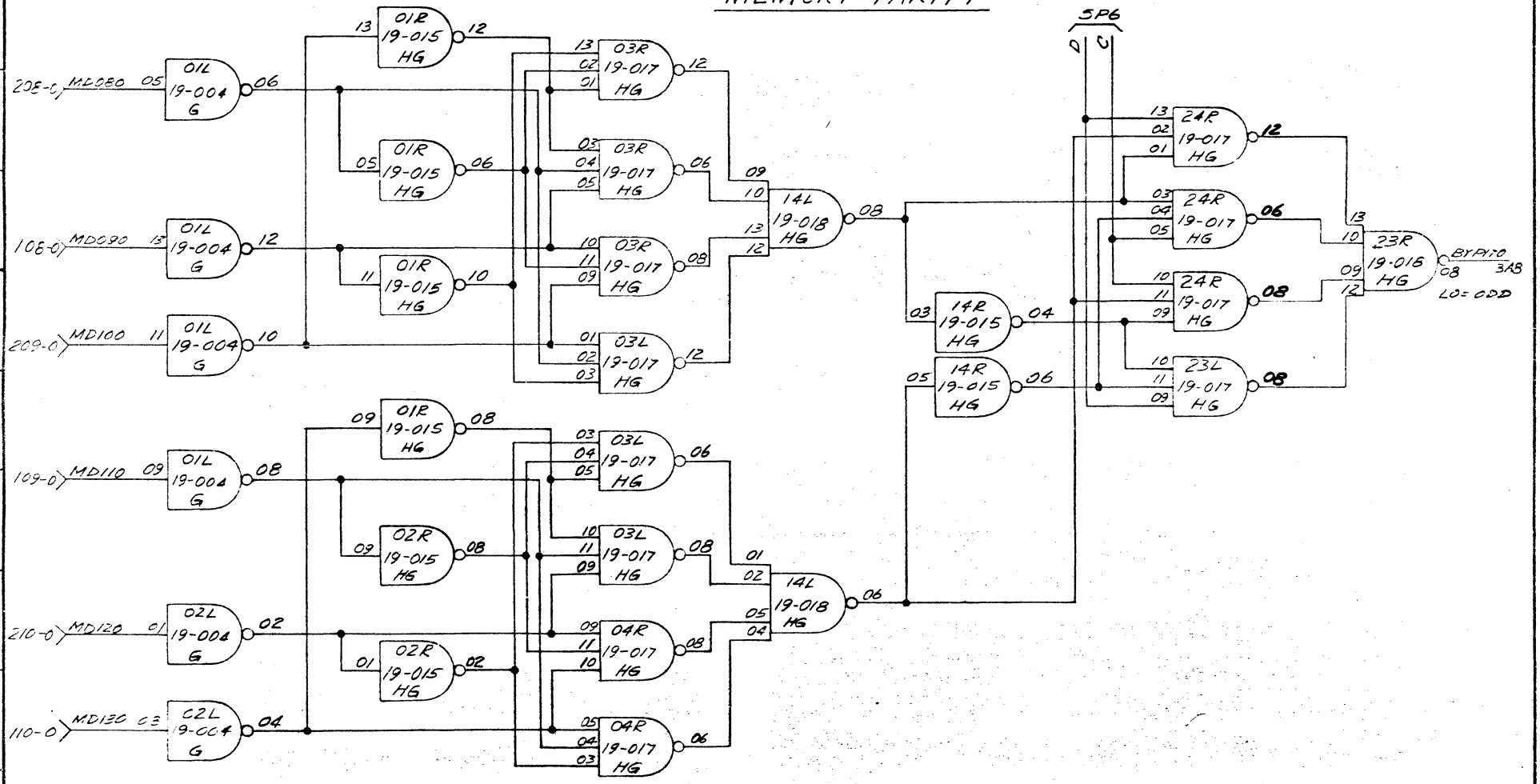
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --
APPLIED PRACTICES | SURFACES | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±
SURFACES: √

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
MEMORY PARITY & PROTECT
FMF GE-PAC 30 | FCF

DWG NO (FS 51) 70B113010
CONT. ON SHEET 5 SH NO 4

MEMORY PARITY



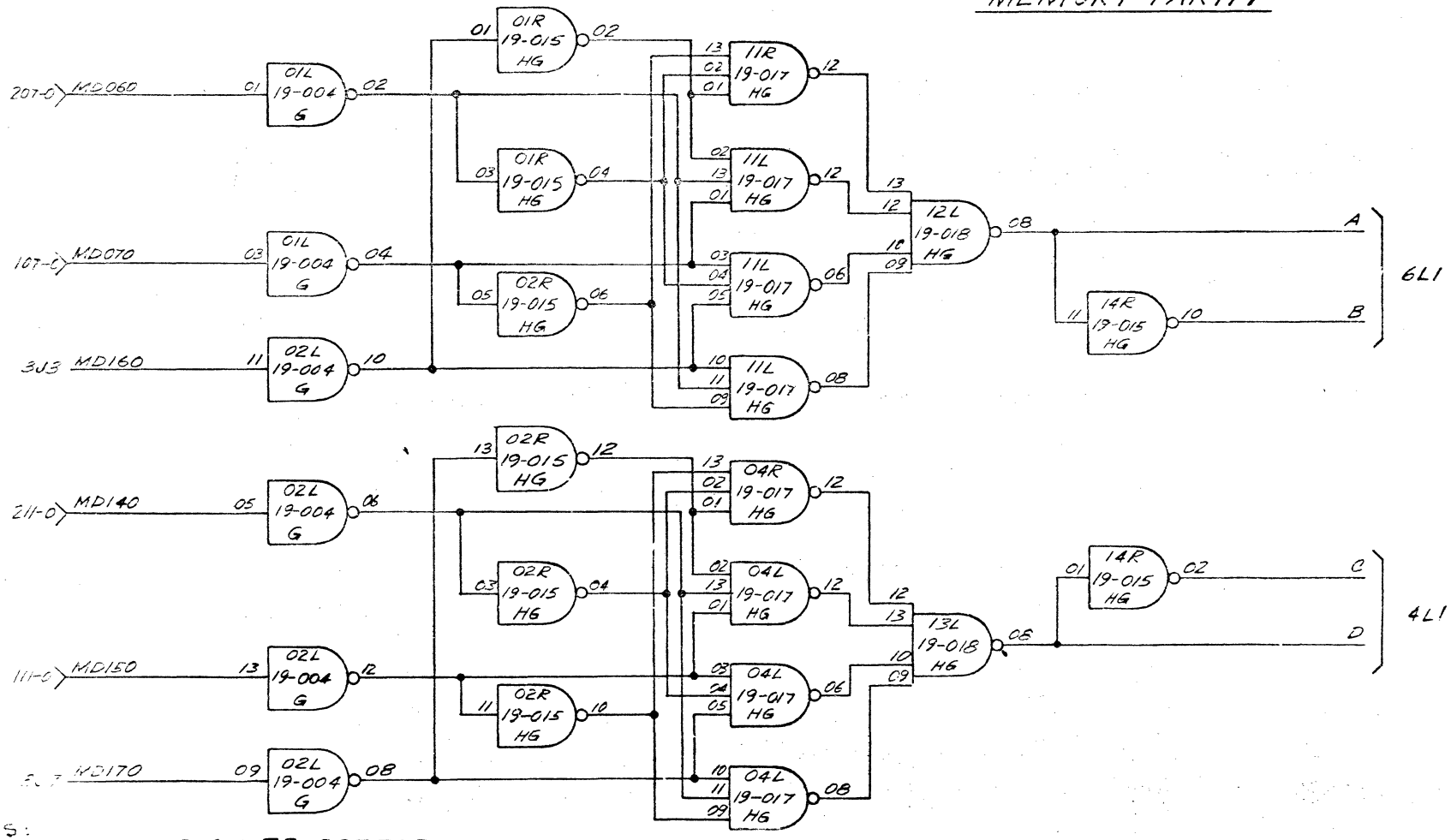
NOTES:
1. DO NOT EQUIP ON 32-087 F02.

MADE BY: M Howard 24 JUNE '69
ISSUED: JUL 18 1969
APPROVAL: E.G. White, June 25, 69
DES.
CHKR. DR
REV. C

DWG. NO. (FS 51) 70B113010
CONT ON SHEET 5 SH NO 4

DIST.	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING — APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES	GENERAL ELECTRIC — PROCESS COMPUTER PHOENIX	TITLE: FUNCTIONAL SCHEMATIC MEMORY PARITY & PROTECT — FMF GE-PAC 30 | FCF	DWG NO. (FS51) 70B113010 — CONT. ON SHEET 6 — SH NO 5
		√	±	±	±			

MEMORY PARITY



NOTES:
1. DO NOT EQUIP ON 32-087F02.

MADE BY	APPROVAL	DES.		REV.		DWG. NO. (FS51) 70B113010
J.S. Howard 24 JUNE '69	E.A. White June 25, 69	CHKR.	DR	C		CONT ON SHEET 6 — SH NO. 5
ISSUED JUL 18 1969						

DIST.

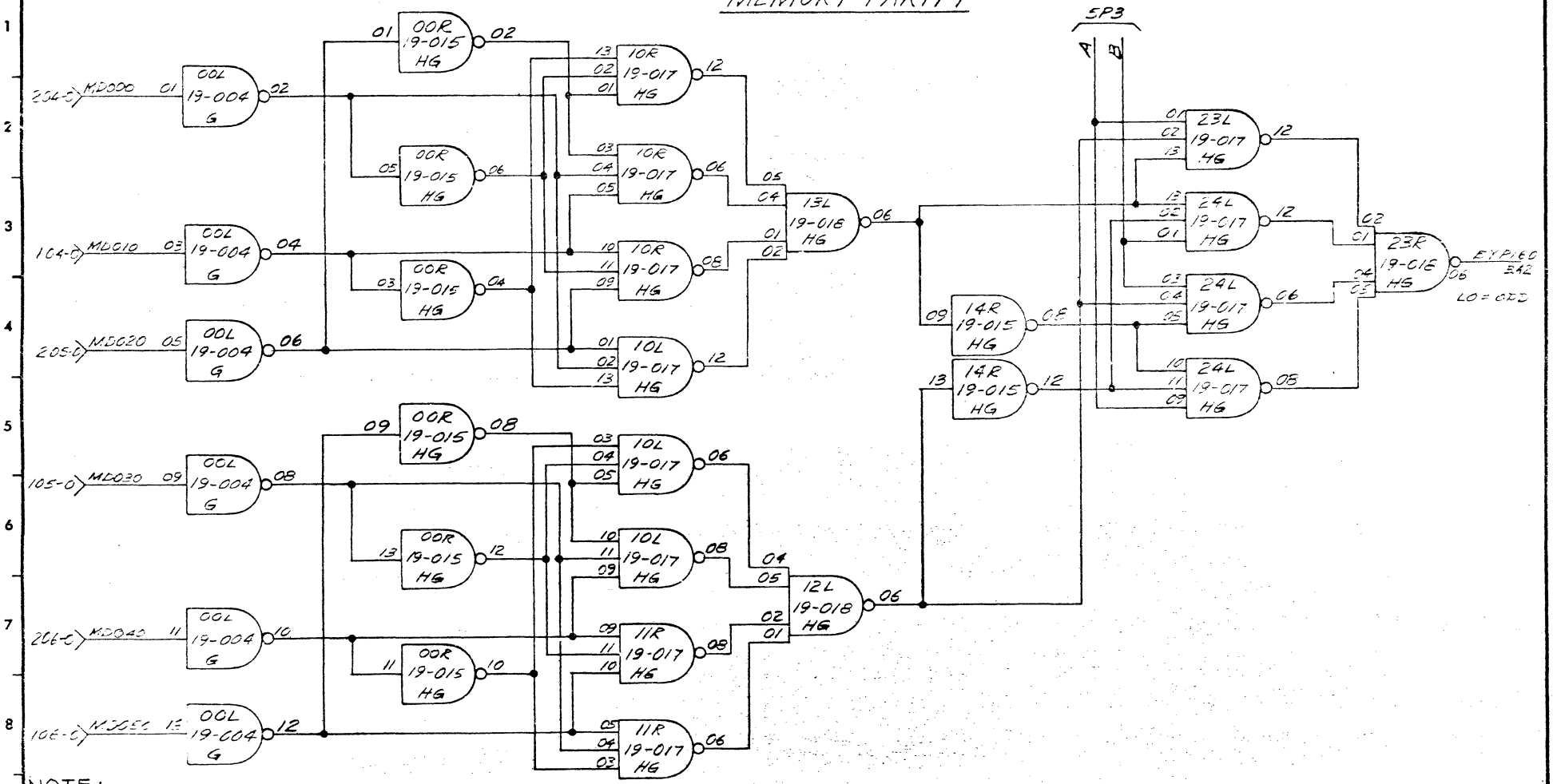
UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING :-
APPLIED PRACTICES | SURFACES | TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± | DECIMALS ± | ANGLES ±
SURFACES: √

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC,
MEMORY PARITY & PROTECT
FMF GE-PAC 30 | FCF

DWG NO (FS51) 70B113010
CONT. ON SHEET 7 SH NO 6

MEMORY PARITY



NOTE:
1- DO NOT EQUIP ON 32-087F02.

MADE BY B.Hammond 24 JUNE '69
ISSUED JUL 18 1969
APPROVAL E.A. White June 25, 69
DES.
CHKR. DR
REV. C

DWG. NO (FS51) 70B113010
CONT ON SHEET 7 SH NO. 6

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC.
MEMORY PARITY & PROTECT
FMF GE-PAC 30 | FCF

DWG NO (FSSI) 70B113010
CONT ON SHEET 8 SH NO 7

A | B | C | D | E | F | G | H | J | K | L | M | N | P | R

1

BACK PANEL MAP

	CONN POS	MOTH. BD	VERT. POS	HORIZ POS 0	1	2	HORIZ POS 0	1	2	HORIZ POS 0	1	2	HORIZ POS 0	1	2	HORIZ POS 0	1	2	HORIZ POS 0	1	2
		MPC	22		P5	GND															
			21																		
			20																		
			19																		
			18																		
			17																		
			16		MA070A	MA060A															
			15		MA050A	MA040A															
			14		MA030A	MA020A															
			13		MA010A	MA000A															
			12																		
			11																		
			10																		
			09																		
			08																		
			07																		
			06																		
			05																		
			04																		
			03																		
			02		OVRAI	PROLO															
			01		STWO	CWRO															
			00		P5	GND															
			22		P5	GND															
			21																		
			20			CPFH															
			19		W50	CPFL															
			18			PFHI															
			17			PLFI															
			16		MBYIA	PFHO															
			15		MDHRO	PFLO															
			14		SPARO	NPARO															
			13		CPARO	SCLRO															
			12		WD170	WD160															
			11		MD150	MD140															
			10		MD130	MD120															
			09		MD110	MD100															
			08		MD090	MD080															
			07		MD070	MD060															
			06		MD050	MD040															
			05		MD030	MD020															
			04		MD010	MD000															
			03		MS170	PPHO															
			02		MS160	PPLO															
			01																		
			00		P5	GND															

1 / 0

MADE BY J. Howard 24 JUNE '69
INSP JUL 18 1969

APPROVAL

DES.
CHKR. DR

REV. C

DWG NO (FSSI) 70B113010
CONT ON SHEET 8 SH NO. 7

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING —

APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS		
		FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC.
MEMORY PARITY & PROTECT
FMF GE-PAC 30 | FCF

DWG. NO. (FSSI) 70B113010
CONT. ON SHEET F SH. NO. 8

BLOCK DIAGRAM

BC15 21-47
BC14 40-47
BC13 11-47
BC12 16 47
BC11 31-47
BC10 30-47
BC09 41-47
BCC8 20-47
CABLE CONNECTOR

GND = NO PROTECT

BCC7 31-46
BCC6 30-46
BCC5 21-46
BCC4 20-46
BCC3 41-46
BCC2 10-46
BCC1 11-46
BCC0 40-46
CABLE CONNECTOR

BLOCK CONTROL LEADS

A7 A6 A5 A4 A3 A2 A1 A0 BUSY

11-07 21-07 31-07 41-07 51-07 61-07 70-07 71-07 20-07

STRAP OPTION BOARD (A)

40-07 50-07 60-07 30-07 10-07

1 OUT OF 16 DECODING

0 1 15

OVERRIDE A (OVRAO)

START OF WRITE (SPARO OR STWO)

CLEAR FLAG (CPRO)

OVERRIDE B

10-44 20-44 11-44 21-44 30-44 41-44 71-44 60-44

ADDRESS RANGE

(B) STRAP OPTION BOARD

70-44 50-44 31-44 41-44 51-44 61-44

IN RANGE

51-46 OVERRIDE B (OVRBO)

EXTERNAL OPTIONS

50-46 PROTECT D.C. (PROLO)
60-46 PROTECT PULSE (PWRO)
70-46 FLAG HI
71-46 FLAG LO
61-46 CLEAR FLAG (CPRO)

FLAG FF S C 1 0

(CWRO) CONVERT WRITE TO READ

(A) CLEAR FLAG FLOP ON END OF BUSY.

(B) OVERRIDE PROTECTION IF OUT OF ADDRESS RANGE. USED FOR EXTENDING NUMBER OF BLOCKS BEYOND 16.

MADE BY S. H. ward 24 JUNE '69
ISSUED JUL 18 1969

APPROVAL E. G. White June 25, 69

DES.
CHKR. DP

REV. C

DWG. NO. (FSSI) 70B113010
CONT ON SHEET F SH NO. 8

GENERAL ELECTRIC

PROCESS COMPUTERS
PHOENIX ARIZONA

TITLE SCHEMATIC DIAGRAM,
POWER SUPPLY - OMI7-A2

DRAWING NUMBER 70B113065 | CONT. 1 | PAGE 0

FIRST MADE FOR GE-PAC 30

(34-002-R01 B08)

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
C	ISSUE				

REISSUED

C	Issued										

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME

REISSUED

(34-002-R01 B08)

MADE BY	APPROVAL	REV.		DWG. NO.	CONT.	PAGE
B. Howard 24 JUNE '69	E. C. White June 26, 69	C		70B113065	1	0
ISSUED July 18, 1969				PRINTS TO:		

PCE 2081

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING. –

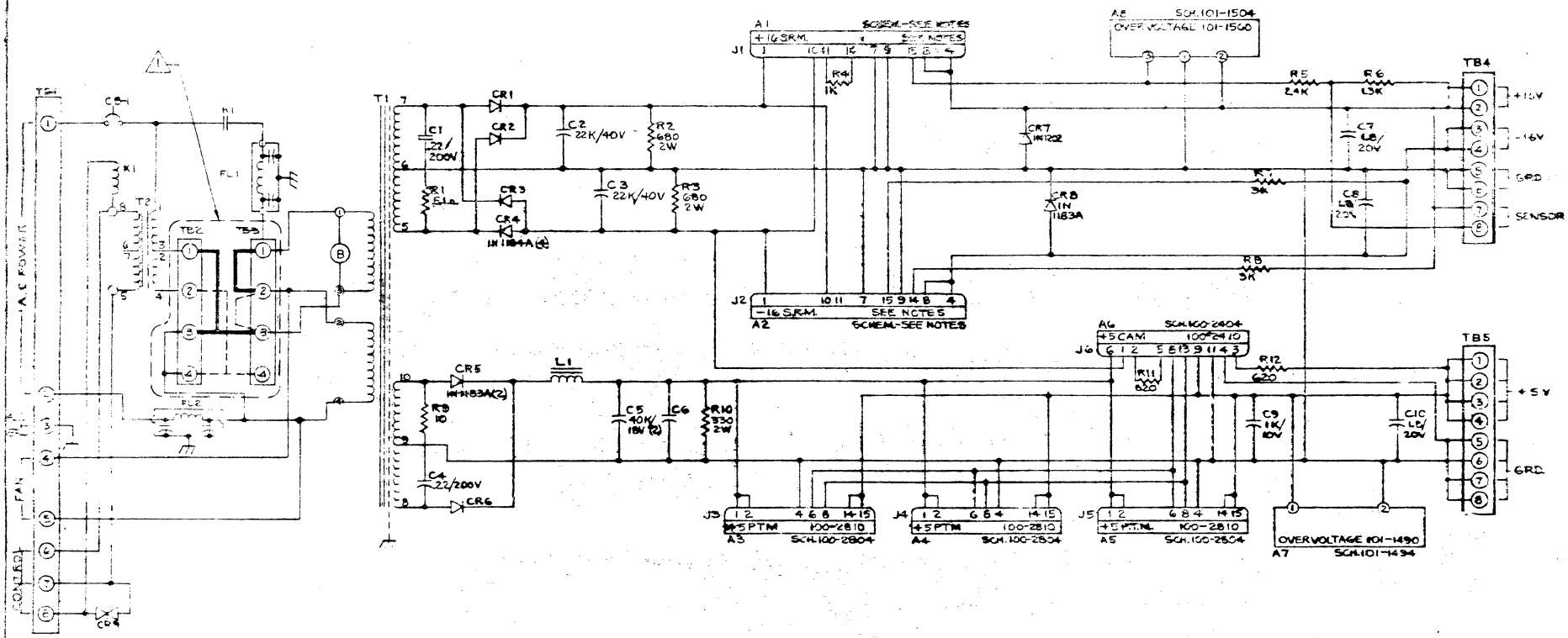
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS		
		FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE SCHEMATIC DIAGRAM,
POWER SUPPY - OM17-A2
FMF GE-PAC 30 | FCF

DWG NO (34-002-R01 B08)
70B113065
CONT. ON SHEET 2 SH NO 1

NOTES:
1. THE SOLID LINE INDICATE THE CONNECTION FOR AN INPUT OF 115 VOLTS. THE DOTTED LINES ARE THE 230 VOLT CONNECTION ALL CONNECTIONS ARE ACCOMPLISHED BY A PRINTED CIRCUIT BOARD WHICH IS CHANGED ONE TERMINAL POSITION TO SWITCH THE INPUT FROM 115 VOLT TO 230 VOLT OPERATION.
2. FOR ASSEMBLY DRAWING SEE 001-0180.



MADE BY
B. Howard 24 JUNE'69

ISSUED JUL 18 1969

APPROVAL
S A White
June 30, 69

DES.

CHKR. DR

REV. C

DWG. NO. (34-002-R01 B08)
70B113065
CONT ON SHEET 2 SH NO. 1

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING:—

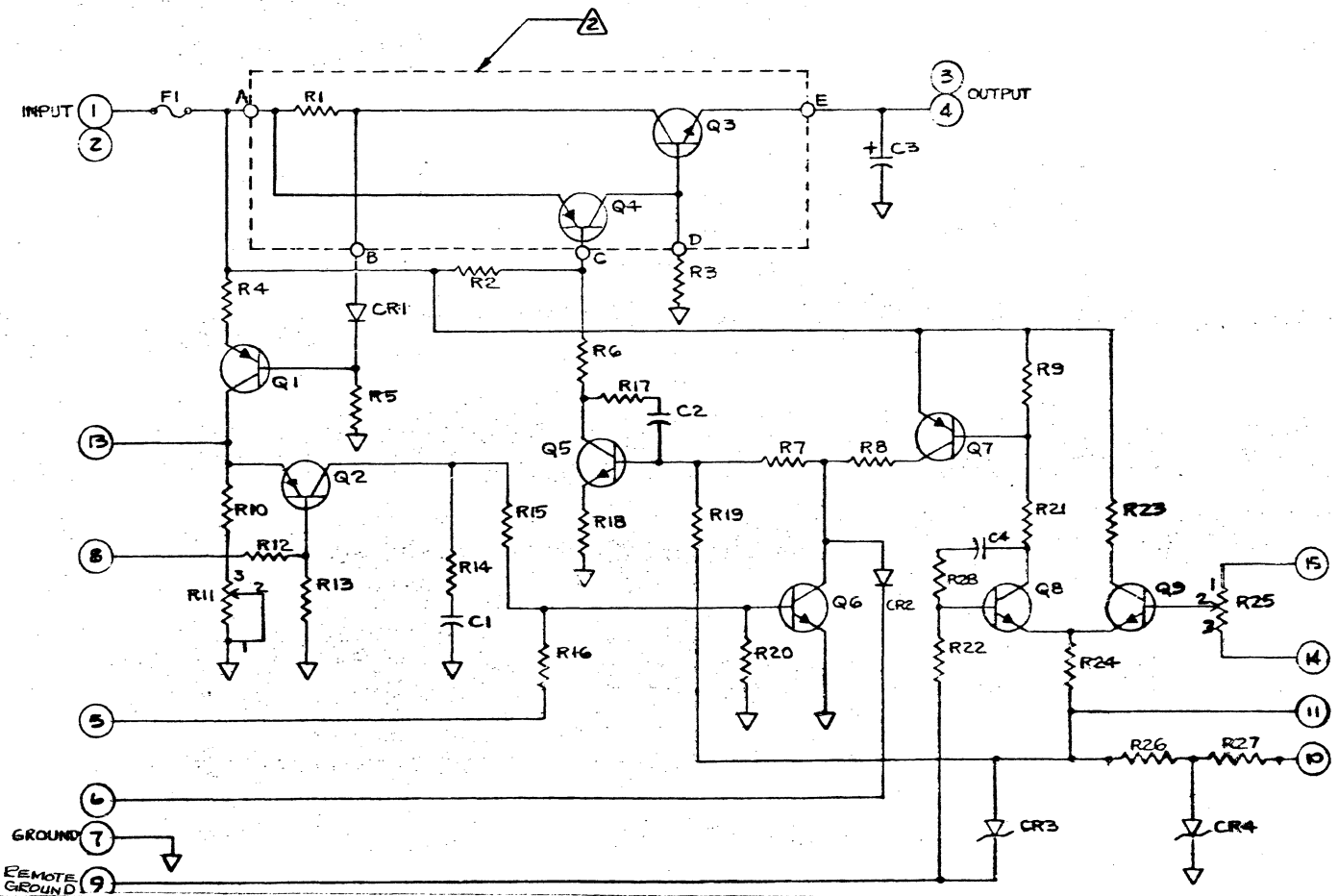
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE SCHEMATIC DIAGRAM,
S.R.M.-PLUS 100-2000 SERIES
FMF GE-PAC 30 | FCF

DWG NO (34-002 R01 B08) 70B113065
CONT ON SHEET 3 SH NO 2

NOTES:
2 -MOUNT INDICATED COMPONENTS ON HEAT SINK 249-0023.
1. FOR MODULE ASSEMBLY SEE DWG. 100-2000.



MADE BY
Edward 24 JUNE '69
ISSUED
JUL 18 1969

APPROVAL
E.A. White
June 30, 69

DES.
CHKR.
REV.

DWG. NO.
70B113065
CONT ON SHEET 3 SH NO. 2

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --

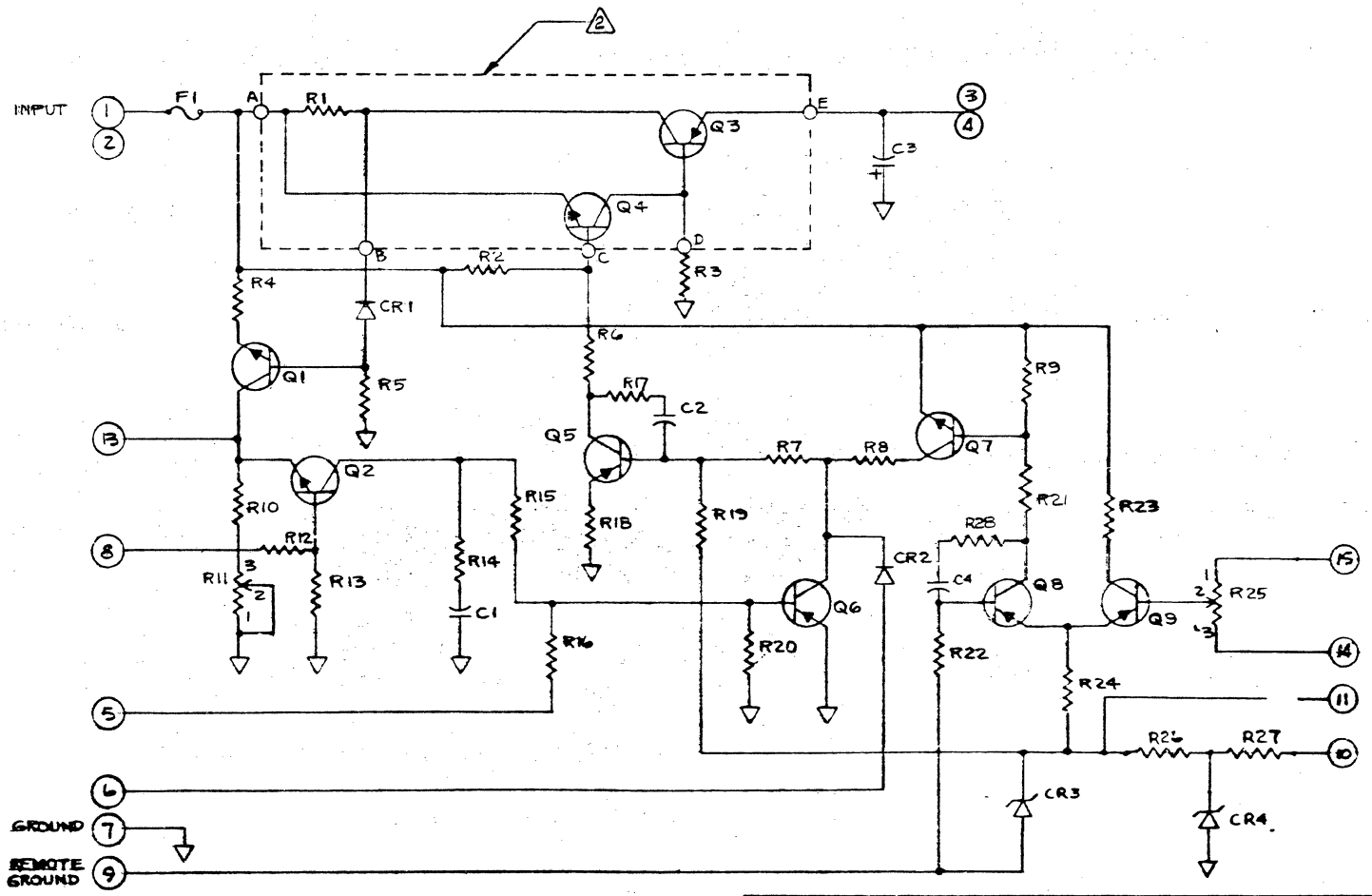
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE SCHEMATIC DIAGRAM,
S.R.M., MINUS 100-2100 SERIES
FMF GE-PAC 30 | FCF

DWG NO (34-002 R01 B08) 70B113065
CONT ON SHEET 4 SH NO 3

NOTES:
2 MOUNT INDICATED COMPONENTS ON HEAT SINK 249-0023
1. FOR MODULE ASSEMBLY SEE DWG. 100-2100.



MADE BY R. Howard 24 JUNE '69
ISSUED JUL 18 1969

APPROVAL E. L. White June 30, 69

DES.
CHKR. DR

REV. C

DWG NO (34-002-R01 B08) 70B113065
CONT ON SHEET 4 SH NO. 3

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --

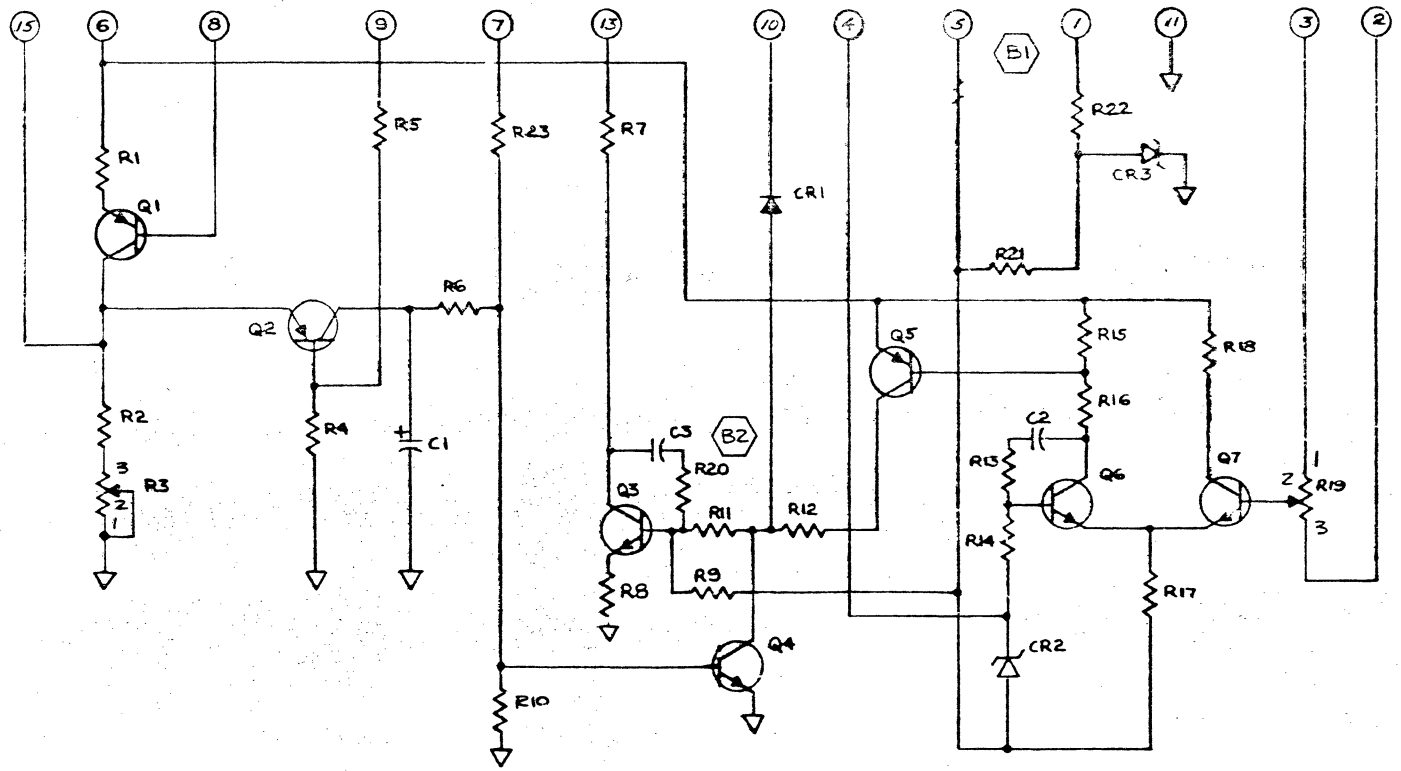
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE SCHEMATIC DIAGRAM,
C.A.M., PLUS 5V. 100-2400 SERIES
FMF GE-PAC 30 | FCF

DWG NO (34-002 R01 B08) 70B113065
CONT ON SHEET 5 SH NO 4

NOTES:
1. FOR MODULE ASSY., SEE DWG. 100-2411.



MADE BY R. Howard 24 JUNE '69
ISSUED JUL 18 1969

APPROVAL E.A. White June 30, 69

DES.
CHKR. OR

REV. C

DWG NO (34-002-R01 B08) 70B113065
CONT ON SHEET 5 SH NO. 4

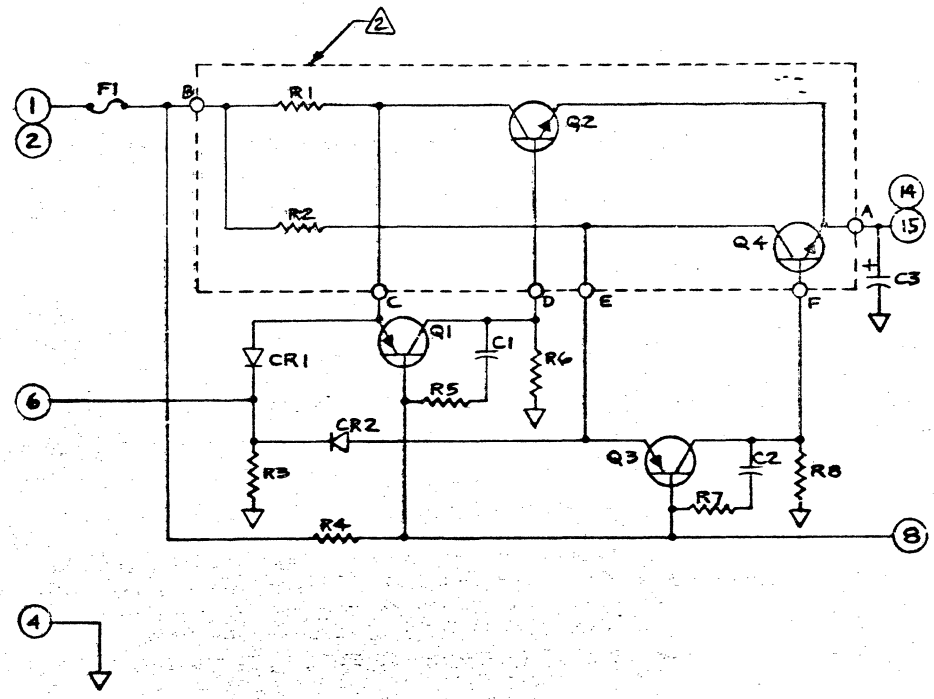
DIST.	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING — APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
		√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE SCHEMATIC DIAGRAM,
P.T.M., PLUS 100-2800 SERIES
FMF GE-PAC 30 | FCF

DWG NO (34-002 R01 B08)
70B113065
CONT. ON SHEET 6 SH NO. 5

NOTES:
2 MOUNT INDICATED COMPONENTS ON HEAT-SINK NO. 242-0024.
1. FOR MODULE ASSEMBLY SEE DWG. NO. 100-2800.



MADE BY	APPROVAL			REV.		DWG. NO. (34-002-R01 B05)
L. Howard 24 JUNE '69	E.A. White June 30, 69	DES.		C		70B113065
ISSUED JUL 18 1969		CHKR.	DR			CONT ON SHEET 6 SH NO. 5

DIST.

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING --

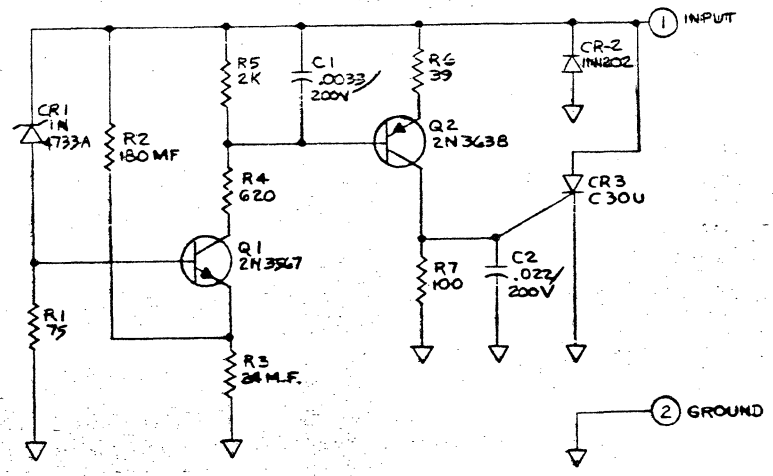
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS		
		FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE SCHEMATIC DIAGRAM,
OVERVOLTAGE I.D.
FMF GE-PAC 30 | FCF

DWG NO (34-002 R01 B08)
70B113065
CONT. ON SHEET 7 SH NO. 6

NOTES:
1. FOR MODULE ASSEMBLY SEE 101-1490.



MADE BY S. Howard 24 JUNE '69
ISSUED JUL 18 1969

APPROVAL E. A. White June 30, 69

DES.
CHKR. DR

REV. C

DWG. NO. (34-002-R01 B08)
70B113065
CONT ON SHEET 7 SH NO. 6

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING —				
APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ±	DECIMALS ±	ANGLES ±
	√			

GENERAL ELECTRIC
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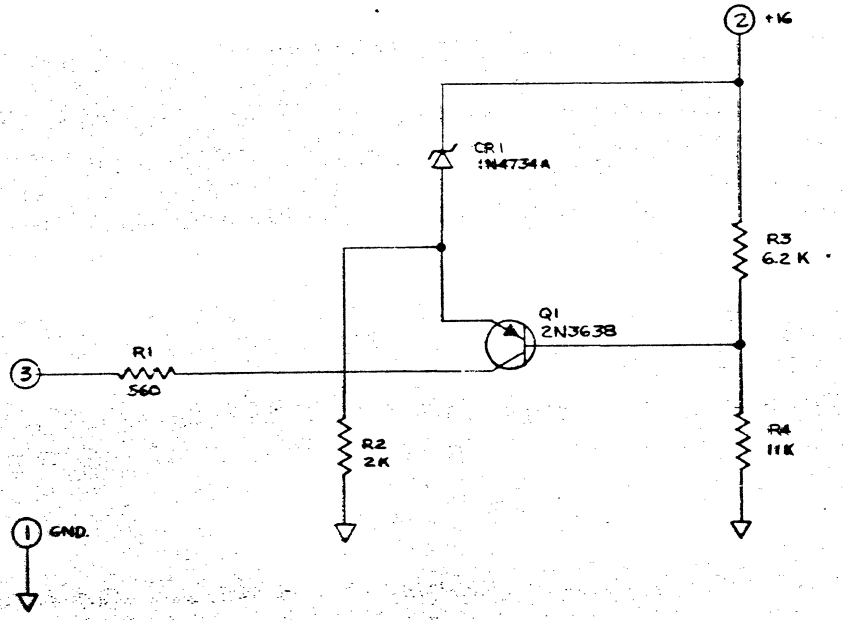
PHOENIX

TITLE SCHEMATIC DIAGRAM,
OVERVOLTAGE ±16
FMF GE-PAC 30 | FCF

DWG NO (34-002 R01 B08)
70B113065
CONT. ON SHEET — SH. NO. 7

NOTES
1. BOARD ASSY. 101-4500



MADE BY B. Howard 24 JUNE '69
ISSUED JUL 18 1969

APPROVAL E. G. White June 30, 69

DES.
CHKR. DR

REV. C

DWG. NO. (34-002-R01 B08)
70B113065
CONT ON SHEET — SH NO. 7

DRAWING NUMBER CONVERSION TABLE

FS2	70B113011
FS3	70B113012
FS4	70B113013
FS5	70B113014
FS28	70B113000
FS29	70B113002
FS44	70B113007
19-001	70A110005
19-002	70A110007
19-003	70A110009
19-004	70A110010
19-005	70A110011
19-006	70A110012
19-007	70A110013
19-008	70A110014
19-012	70A110015
19-014	70A110016
19-015	70A110017
19-016	70A110022
19-017	70A110023
19-018	70A110001
19-019	70A110003
32-009-R02	70A110272
32-010	70A110273
32-010 F01	70A110274
32-011 R01	70A110277
32-012 R01	70A110278
32-013 R01	70A110280
32-014 R01	70A110282
32-017 R03	70A104048 P3
32-017 F01 R05	70A104048 P5
32-017 F02	70A104048 P1
32-017 F03	70A110284
32-017 F04	70A110285
32-017 F05 R02	70A110286
32-041 R01	70A110310
32-043 R01	70A110379
32-044 R02	70A110316
32-061 R01	70A110335
32-062	70A110049
32-062 F01 R01	70A110336
32-062 F02	70A110337
32-063	70A110338
32-068 R01	70A110345
32-068 F01	70A110346
32-074 R02	70A110352
32-075 R05	70A110353
32-076 R07	70A110354
32-077 R10	70A110355
32-087	70A110367
32-087 F01	70A104048 P10
32-087 F02	70A110368

DRAWING NUMBER CONVERSION TABLE
(CONT.)

35-001	70A110382 P1
35-002	70A110382 P2
35-003	70A110382 P3
35-008	70A110382 P9
35-009	70A110382 P10
35-014	70A110382 P14
35-016	70A110382 P16
35-020	70A110382 P20
35-022	70A110382 P22
35-024	70A110382 P24
35-027	70A110382 P27
35-036	70A110382 P39
35-041	70A110382 P45
35-053	70A110382 P54
35-054	70A110382 P58
35-055	70A110382 P59
35-056	70A110382 P60
35-059	70A110382 P62
35-060	70A110382 P63
35-063	70A110382 P66
35-064	70A110382 P67
35-082	70A110382 P73
35-083	70A110382 P74
35-092 R01	70A110382 P167
35-094 R02	70A110382 P84
35-096	70A110382 P85
35-096 F01	70A110382 P86
35-115	70A110382 P106
35-116	70A110382 P107
35-117	70A110382 P108
35-118	70A110382 P109
35-119	70A110382 P110
35-126	70A110382 P120

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